

# Video broadcast JPEG2000 decoder

BA108DVBJPEG2000D factsheet

## Features

- Compliant with JPEG2000 (ISO/IEC 15444-1)
- Integrated Intellectual Property core offering a complete FPGA solution for video broadcast JPEG2000
- Single-chip FPGA solution for full HD 1080p
- Flexible resolution adjustment: configurable to any frame size up to 1920x1080
- Input bit rate: up to 250 Mbits/s
- YUV 4:2:2 color space
- Supported decoder parameters:
  - CPRL progression order, single layer
  - Wavelet filter type: 9/7
  - Number of wavelet decompositions: 0 to 6 levels
  - Full-frame decoding (no tiling)
  - Pixel depth: 12 bits
  - Code block size: 32x32 samples
- Fully autonomous decoder with automatic parameter extraction
- Minimal user intervention
- Fully synchronous design
- Can be used for FPGA, ASIC and Structured ASIC technologies
- Can be integrated with Barco Silex cryptography cores (AES) for advanced security
- Customizable to other high-performance applications or other parameter sets

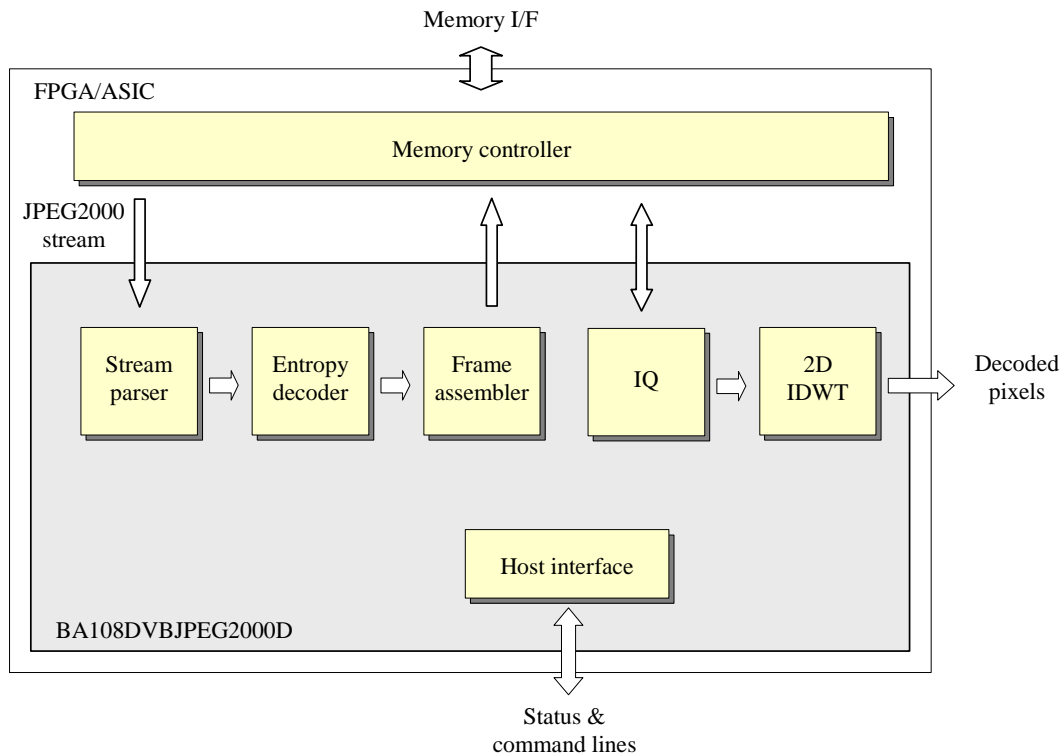


Figure1

Version: 2.1

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## General description

Capitalizing on its long-term experience with JPEG2000 hardware coding, Barco Silex has extended its JPEG2000 portfolio by releasing a new smaller real-time hardware decoder engine that is optimized for digital video broadcast applications. The core architecture offers a flexible and high-speed solution to the performance challenges of broadcast and post-production applications. It is able to sustain the high decoding requirements of such applications, with full HD 1080p resolution and frame rates of 60 Hz.

The BA108DVBJPEG2000D IP core is a JPEG2000 hardware decoder dedicated to digital video broadcast. It decodes streams compliant with the ISO/IEC 15444-1 specification (JPEG2000). It applies JPEG2000 decoding on un-tiled large color frames with 4:2:2 YUV color space.

The core performs the complete video decompression operations: the stream parsing and header decoding, the entropy decoding, inverse quantization and inverse discrete wavelet transform (IDWT). It expects a JPEG2000 compliant file at its input interface and generates decoded 4:2:2 YUV samples at its output interface.

The core is optimized for speed and is able to deal with the demanding broadcast processing speed: it is able to provide a single-chip and single-core FPGA solution for full HD 1080p video streams. The flexible FPGA architecture allows the user to build a secure decoder by integrating Barco Silex cryptography decoders (AES).

## Applications

- Digital video broadcasting.
- Post-production.
- The core can also be integrated in a variety of other applications with similar high-demanding processing requirements. The underlying architecture of the core enables a broad range of features and performance options, as well as specific customizations.

## Technical description

Figure 1 illustrates a simplified block diagram of the BA108DVBJPEG2000D IP showing the internal modules and the interfaces. The BA108DVBJPEG2000D IP is a hardware engine performing the complete JPEG2000 decoding process, taking compliant JPEG2000 streams at its input interface and generating raw pixels at its output interface (separated in their YUV color constituents). The core recomposes a complete frame without any tiling.

The IP core features 3 main interfaces: a pixel interface, a control interface and a memory interface for intermediate large data storage and stream parsing. The decoder control interface allows the user to trigger decoding and to monitor the status of the decoding process.

The decoder requires a single external memory containing the JPEG2000 files to decode and intermediate buffered data. The core implements these memory channels as a generic multi-port interface to a memory controller. This will typically be a DDR SDRAM controller.

The memory requirements for the IP are as follows:

Version	SDRAM size
HD (1920x1080p)	64 MB

The following sections describe the modules constituting the BA108DVBJPEG2000D core as depicted under Figure 1.

### JPEG2000 stream parser

This module analyses the headers, unpacks the compressed data and sends them to the entropy decoding unit.

## Entropy decoder (modeler and arithmetic decoder)

This module gets compressed coding passes from the parser and converts them to quantized code blocks. The Modeler gives the sequencing of the entropy decoding: it reconstructs the code block bit plane by bit plane from most significant to least significant and places relevant bits in zigzag order in each bit plane. Moreover it computes the context information needed by the arithmetic decoder.

The contexts and the bit stream provided by the parser are processed by the Arithmetic Decoder that generates the decoded bits placed at the right location by the Modeler.

## Frame assembler

This unit reconstructs subbands based on the code blocks coming from the entropy decoding channels. This is done by writing the decoded codeblocks into the external memory at the right location inside the subband they belong to.

## Inverse quantizer

The inverse quantizer applies an inverse quantization step as specified in the stream header. A different inverse quantization step is available for each subband resulting in differently weighted frequency subbands. The quantization steps are extracted from the JPEG2000 file headers by the header parser.

## 2D IDWT

This module performs the inverse 2D wavelet transform. It is able to process frames without tiling (with a size up to 4096x2160). It performs wavelet recomposition on the subbands situated in the off-chip tile buffer with a programmable number of decomposition levels up to 6, as specified in the stream header. The wavelet transform is the 9/7 filter with increased compression efficiency.

## Host interface

This interface provides status and command lines at the disposal of the user. These are used to trigger decoding of JPEG2000 files and to follow the status of the decoding process. The user intervention is minimized and the core has a completely autonomous behaviour.

## Memory controller (option)

The JPEG2000 decoding core needs external memory to store temporary intermediate data to ensure smooth and efficient processing of the compressed video stream. This is achieved by using DDR SDRAM. The JPEG2000 decoder IP core interfaces with the memory controller through an easy generic multi-port interface allowing the user to implement his own memory controller and to adapt the decoding architecture to the exact board topology. A dedicated memory controller can also be purchased separately as an option to the BA108DVBJPEG2000D IP core.

## Implementation data

The following table is a summary of device requirements and related decoding performance for both Xilinx and Altera FPGAs. The table shows possible resolutions and frame rates for the listed devices. This table is based on an illustrative compressed bit rate of 250Mbps

Vendor	Device *	Resolution	Frame rate
Altera	EPS2S90	HD 1080p	60 fps
Xilinx	XC5VLX110T	HD 1080p	60 fps

\* Listed devices contain enough free logic and memory blocks to implement additional functions (e.g. memory controller, AES decryption,...)

The core can be configured for higher resolutions or higher bit rates. It can also be configured to support other JPEG2000 parameters sets. For more information please contact [barco-silex@barco.com](mailto:barco-silex@barco.com).

## Barco Silex overview

Barco Silex has acquired worldwide expertise in advanced image processing and security applications for digital cinema, broadcasting, surveillance, printing, aerospace, secure payment... Combining high-end know-how in image and video processing and custom design capabilities (ASIC/FPGA/DSP/IP), the company delivers high-grade custom-built video processing solutions.

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group. It has 15 years of industrial experience in the ASIC and FPGA markets and offers you long term support and continuity.

## Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

## More information

Order-reference: **BA108DVBJPEG2000D**

A dedicated memory controller can also be ordered separately as an option. Cryptography cores (AES) are also available and can be ordered separately.

For additional information and other IP products contact:

Barco – Silex

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