

BA109 HD/DCI JPEG 2000 Decoder

Factsheet

Features

- **Multi-channel HD**
- **Compliant with DCI (Digital Cinema Initiatives) recommendation**
- Compliant with JPEG 2000 (ISO/IEC 15444-1)
- Integrated Intellectual Property core offering a full FPGA solution for HD and DCI JPEG 2000
- Single-chip FPGA solution for multi-channel:
 - DCI: 2K @24fps, 2K @48fps and 4K @24fps
 - HD: 720p30/60, 1080i, 1080p30/60
 - Custom frame sizes up to 4096x2160
- Customizable input bit rate: up to 250 Mbps / 500 Mbps / 1 Gbps / lossless
- XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces with support for ICT/RCT color transform
- Supported decoder parameters:
 - Wavelet filters: 9/7 and 5/3, 0 to 6 levels
 - Full-frame decoding (no tiling)
 - Pixel depth: up to 12 bits per color sample (lossless mode up to 16 bits)
 - Code block size: 32x32 samples
 - CPRL / LRCP progression orders
- Fully autonomous decoder with automatic parameter extraction, minimal user intervention
- Fully synchronous design
- Can be used for FPGA, ASIC and Structured ASIC technologies
- Can be integrated with Barco Silex cryptography cores (AES) for advanced security

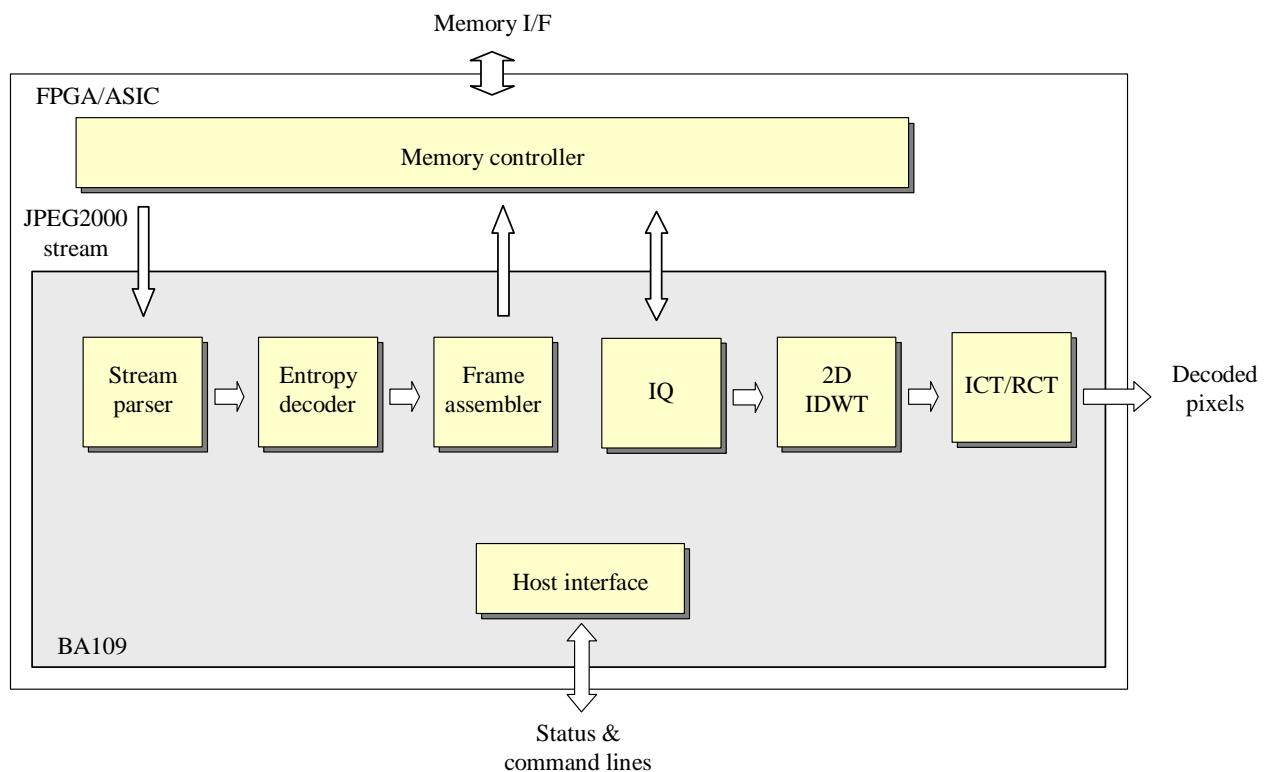


Figure1

General description

Capitalizing on its long-term experience with JPEG 2000 hardware coding, Barco Silex has extended its JPEG 2000 portfolio by releasing a new compact real-time hardware decoder engine that is optimized for Digital Cinema and High-Definition video applications. The core architecture offers a flexible and high-speed solution to the performance challenges of cinema, broadcast and post-production applications. It is able to sustain the high decoding requirements of the large DCI frame formats, including 4096x2160 resolution and frame rates up to 48 frames per second.

The BA109 IP core is a JPEG 2000 hardware decoder dedicated to DCI (Digital Cinema Initiatives) and HD video applications. It decodes streams compliant with the ISO/IEC 15444-1 specification (JPEG 2000). It is compliant with the DCI recommendation for video coding. It applies JPEG 2000 decoding on un-tiled large color frames with 4:4:4 or 4:2:2 color resolutions.

The core performs the complete video decompression operations of the normalized decoding process: stream parsing and header decoding, entropy decoding, inverse quantization, inverse discrete wavelet transform (IDWT) and inverse color transform (ICT/RCT). It supports a JPEG 2000 j2c file at its input interface and generates decoded samples at its output interface under the following formats: 4:4:4 or 4:2:2 color resolutions with 12-bit samples (up to 16-bit samples in lossless mode).

The core is optimized for speed and is able to deal with the demanding DCI and HD processing speeds: it is able to provide a single-chip FPGA solution for all 2K @24 fps, 2K @48fps, 4K @24fps, 720p30/60, 1080i and 1080p30/60 distributions. The flexible FPGA architecture allows the user to build a secure decoder by integrating Barco Silex cryptography decoders (DCI AES).

Applications

- Digital cinema video decoding, following DCI recommendation.
- Digital video broadcasting, contribution.
- Post-production.
- Video archiving and projection.
- Wireless video.
- The core can also be integrated in a variety of other applications with similar high-demanding processing requirements. The underlying architecture of the core enables a broad range of features and performance options, as well as specific customizations.

Technical description

Figure 1 illustrates a simplified block diagram of the BA109 IP showing the internal modules and the interfaces. The IP core features 3 main interfaces: a pixel interface, a control interface and a memory interface for intermediate large data storage and stream parsing. The decoder control interface allows the user to trigger decoding and to monitor the status of the decoding process.

The decoder requires a single external memory containing the JPEG 2000 files to decode and intermediate buffered data. The core implements these memory channels as a generic multi-port interface to a memory controller. This will typically be a DDR/DDR2 SDRAM controller.

The memory requirements for the IP are as follows:

Version	SDRAM size
2K (24fps/48fps)	64 MB
HD (1920x1080)	64 MB
4K	256 MB

The following sections describe the modules constituting the BA109 core as depicted under Figure 1.

JPEG 2000 stream parser

This module analyses the headers, unpacks the compressed data and sends them to the entropy decoding unit.

Entropy decoder (modeler and arithmetic decoder)

This module gets compressed coding passes from the parser and converts them to quantized code blocks. The Modeler gives the sequencing of the entropy decoding: it reconstructs the code block bit plane by bit plane from most significant to least significant and places relevant bits in zigzag order in each bit plane. Moreover it computes the context information needed by the arithmetic decoder. The contexts and the bit stream provided by the parser are processed by the Arithmetic Decoder that generates the decoded bits placed at the right location by the Modeler.

Frame assembler

This unit reconstructs subbands based on the code blocks coming from the entropy decoder. It outputs decoded codeblocks into the external memory at the right location inside the subband they belong to.

Inverse quantizer

The inverse quantizer applies an inverse quantization step as specified in the stream header. A different inverse quantization step is available for each subband resulting in differently weighted frequency subbands. The quantization steps are extracted from the JPEG 2000 file headers by the header parser.

2D IDWT

This module performs the inverse 2D wavelet transform. It is able to process frames without tiling (with a size up to 4096x2160). It performs wavelet recomposition on the subbands situated in the off-chip buffer with a programmable number of decomposition levels up to 6, as specified in the stream header. Both 9/7 and 5/3 filters are supported.

ICT/RCT

If enabled, this unit performs the irreversible or reversible color transform on the samples generated by the wavelet transform. This optional operation converts samples from YUV to RGB. It is used to further improve the compression efficiency. The ICT/RCT module generates reconstructed samples of any size up to 12 bits (up to 16 bits in lossless mode). The color transform operation is automatically activated by the header decoder.

Host interface

This interface provides status and command lines at the disposal of the user. These are used to trigger decoding of JPEG 2000 DCI files and to follow the status of the decoding process. User intervention is minimized as the core has a completely autonomous behavior.

Memory controller (option)

The JPEG 2000 decoding core uses external memory to store temporary intermediate data to ensure smooth and efficient processing of the video stream. This is achieved by using DDR/DDR2 SDRAM. The JPEG 2000 decoder IP core interfaces with the memory controller through an easy generic multi-port interface allowing the user to implement his own memory controller and to adapt the decoding architecture to the exact board topology. A dedicated memory controller can also be purchased separately as an option to the BA109 IP core.

Implementation technologies

The BA109 JPEG 2000 decoder is compact and fast, reaching speeds suitable for HD video and DCI. It is also flexible and can be provided for different FPGA families and ASIC technologies. We commit to continuously keep our cores at a state-of-the-art optimization level for the newest FPGA devices on the market. We offer solutions for Xilinx Virtex4, Virtex5, Spartan3 and Altera StratixII, StratixIII, StratixIV and CycloneIII devices. Please contact us for implementation data.

Depending on the selected technology, we are able to provide the BA109 core for various configurations and speeds: up to 2K @96 fps, up to 4K @24 fps, up to 1080p @120 fps, at 250Mbps / 500Mbps / 1Gbps / lossless bandwidths. The BA109 core can also be used in 3D or even multi-stream modes where several streams are decoded at the same time.

Barco Silex overview

Barco Silex has world-class expertise in advanced image processing and security applications for digital cinema, broadcasting, surveillance, printing, aerospace, secure payment... Combining high-end know-how in image and video processing and custom design capabilities (ASIC/FPGA/DSP/IP), the company delivers high-grade custom-built video processing solutions.

Barco Silex is a microelectronics design house located in Belgium and France belonging to the Belgian Barco group. It has 15 years of industrial experience in the ASIC and FPGA markets and offers you long term support and continuity.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order reference: please contact us for order reference, depending on selected core synthesis options.

A board-based demo setup and evaluation kit is available and can be ordered separately as an option.

A dedicated memory controller can also be ordered separately.

Cryptography cores (AES) are also available and can be ordered separately.

For additional information and other IP products contact:

Barco – Silex

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