

JPEG 2000 Encoder Multi-channel HD/DCI

BA110 - Factsheet

Features

- **Compliant with JPEG 2000 (ISO/IEC 15444-1)**
- **Multi-channel interface**
- **Compliant with DCI (Digital Cinema Initiatives) recommendation**
- Integrated Intellectual Property (IP) core for HD and DCI JPEG 2000
- Single-FPGA solution for multi-channel:
 - DCI: 2K@24fps, 2K@48fps, 2K3D@24fps, 4K@24fps and 4K3D@24fps
 - HD: 720p30/60, 1080i, 1080p30/60
 - Custom frame sizes up to 4096x2160
- Customizable output bit rate: up to 250Mbps / 500Mbps / 1Gbps / lossless
- XYZ, RGB, YUV (4:4:4 or 4:2:2) color spaces with support for ICT/RCT color transform
- Supported JPEG 2000 parameters:
 - Wavelet filters: 9/7 and 5/3, 0 to 6 decomposition levels
 - Full-frame encoding (no tiling)
 - Pixel depth: up to 12 bits per color sample
 - Configurable bit rate on a frame by frame basis with 3 selectable regulation modes
 - Quality: quantization, weights, ...
- Minimal user intervention
- Fully synchronous design
- Can be used for FPGA, ASIC and Structured ASIC technologies
- Can be integrated with Barco Silex cryptography cores (AES) for advanced security

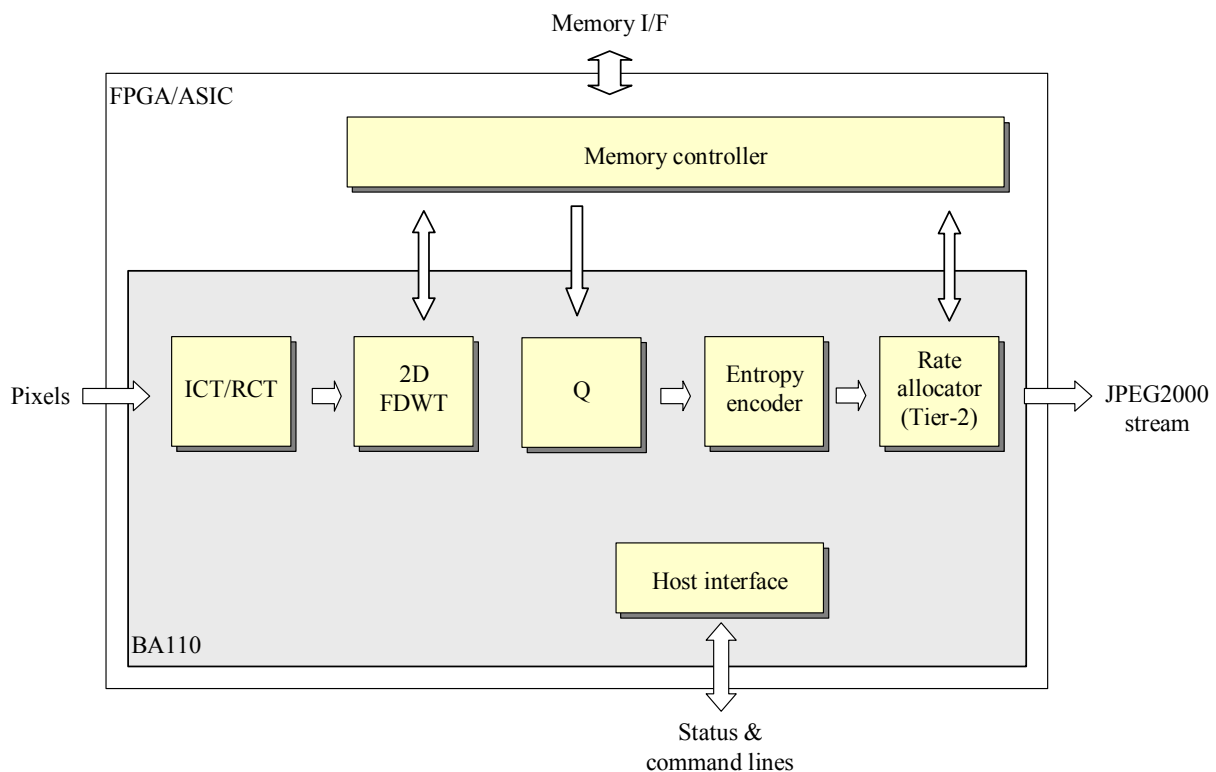


Figure1

General description

Capitalizing on its long-term experience with JPEG 2000 hardware coding, Barco Silex offers a large JPEG 2000 portfolio including this compact real-time hardware encoder engine that is optimized for Digital Cinema (DCI) and High-Definition (HD) video applications. The core architecture offers a flexible and high-speed solution to the challenges of digital cinema, broadcast and post-production applications. The BA110 is able to sustain the high encoding requirements of the large DCI frame formats, including 4096x2160 resolution and frame rates up to 48 frames per second.

The BA110 IP core is a JPEG 2000 hardware encoder dedicated to DCI (Digital Cinema Initiatives) and HD video applications. It performs the JPEG 2000 encoding of large un-tiled color frames with 4:4:4 or 4:2:2 sub-sampling. The BA110 generates compressed streams compliant with the ISO/IEC 15444-1 specification (JPEG 2000).

The IP core performs the following video compression operations of the normalized encoding process:

- Color transform (ICT/RCT)
- Discrete wavelet transform (DWT)
- Quantization
- Entropy encoding
- Rate allocation

The BA110 accepts pixels on its input interface with up to 12 bits per color components. It generates a j2c JPEG 2000 stream at its output interface.

The core is optimized for speed and is able to deal with the demanding DCI and HD processing requirements: it is able to provide a single-chip FPGA solution for all 2K@24 fps, 2K@48fps, 2K3D@24fps, 4K@24fps, 4K3D@24fps, 720p30/60, 1080i and 1080p30/60 resolutions.

The flexible FPGA architecture allows the user to build a secure encoder by integrating Barco Silex cryptography products (DCI AES).

Applications

- Digital cinema video coding (following DCI recommendation)
- Digital video broadcasting, contribution
- Post-production
- Video mastering, archiving and acquisition
- Wireless video.

The BA110 JPEG 2000 encoder can also be integrated in a variety of other applications with similar high-demanding processing requirements. The underlying architecture of the core enables a wide range of features and performance options, as well as specific customizations.

Technical description

Figure 1 illustrates a simplified block diagram of the BA110 IP showing the internal modules and the interfaces. The IP core features 4 main interfaces: a pixel interface, a stream interface, a control interface and a memory interface for intermediate large data storage. The encoder control interface allows the user to parameter the core, trigger encoding and monitor the status of the encoding process.

The encoder requires a single external memory containing intermediate buffered data. The core implements these memory channels as a generic multi-port interface to a memory controller. This will typically be a DDR2/DDR3 SDRAM controller.

The memory requirements for the IP are as follows:

Version	SDRAM size
2K (24fps/48fps)	96 MB
HD (1920x1080)	96 MB
4K	384 MB

The following sections describe the modules constituting the BA110 core as depicted under Figure 1.

ICT/RCT

If enabled, this unit performs the irreversible or reversible color transform on the input samples. This optional operation converts samples from RGB to YUV space. It is used to provide better decorrelation of the color components and thus increase the compression efficiency. The ICT/RCT module accepts samples of any size up to 12 bits (16 bits in lossless mode). The color transform operation is enabled by the user.

2D FDWT

This module performs the forward 2D wavelet transform. It is able to process frames without tiling (with a size up to 4096x2160). It performs wavelet decomposition with a programmable number of decomposition levels (up to 6), as specified by the user. Both 9/7 (lossy) and 5/3 (lossless) filters are supported. The wavelet engine stores its temporary result in the external memory.

Quantizer

The quantizer applies quantization steps as specified by the user. A different quantization step is programmable for each subband resulting in differently weighted frequency subbands. This unit also divides the decomposed subbands into code blocks and dispatches the various code blocks to the entropy encoding channels. This is done by reading the code blocks from the external memory at the appropriate location inside the subband they belong to.

Entropy encoder (modeler and arithmetic encoder)

This module generates compressed coding passes (JPEG 2000 codestream) from the quantized code blocks it receives from the quantizer. The Modeler gives the sequencing of the entropy encoding: it decomposes the code block bit plane by bit plane from most significant to least significant and places relevant bits in zigzag order in each bit plane. Moreover, it computes the context information needed by the arithmetic encoder. The contexts and binarized code blocks are processed by the Arithmetic Encoder that generates the bit stream ready to be encapsulated in a JPEG 2000 file.

Rate allocator

This module performs optimal rate allocation based on the metrics information produced by the entropy encoder, for the purpose of constraining the generated bit rate. This module also embeds the generated codestream in a JPEG 2000 file container ready for decoding by any 3rd party JPEG 2000 decoder. The rate allocator is configured by the user to target one of the 3 supported rate-control modes: constant quality, constant bit rate, constant quality with maximum bitrate. The user can select the rate-control mode on a frame-by-frame basis.

Host interface

This interface provides configuration, status and command lines at the disposal of the user. It is used to parameterize the JPEG 2000 process, trigger encoding of a JPEG 2000 picture and to follow the status of the encoding process. User intervention is minimized.

Memory controller

The JPEG 2000 encoding core uses external memory to store temporary intermediate data to ensure smooth and efficient processing of the video stream. This is usually achieved by using DDR2/DDR3 SDRAM. The JPEG 2000 encoder IP core interfaces with the memory controller through an easy generic multi-port interface allowing the user to adapt the encoding architecture to the exact board topology.

Implementation technologies

The BA110 JPEG 2000 encoder is compact and fast, reaching speeds suitable for HD video and DCI. It is also flexible and can be provided for different FPGA families and ASIC technologies. We commit to continuously keep our cores at a state-of-the-art optimization level for the newest FPGA devices on the market. We offer solutions for Xilinx Virtex-6, Virtex-5, Spartan-6 and Altera Stratix-4, Stratix-3, Arria-2GX and Cyclone-4 devices.

Please contact us for detailed implementation data.

Depending on the selected technology, we are able to provide the BA110 core for various configurations and speeds: up to 2K@96fps, up to 4K@24 fps, up to 1080p@120fps, at 250Mbps / 500Mbps / 1Gbps / lossless bandwidths. The BA110 core can also be used in 3D or even multi-stream modes where several streams are compressed at the same time.

Barco Silex overview

Barco Silex is a leader in contract engineering services, custom hardware and software development, as well as Intellectual Property (IP). Its high quality JPEG 2000 IP cores, developed since 2002, are optimized for all leading-edge FPGAs as well as for legacy platforms.

Thanks to its continued stream of aggressive innovations, Barco Silex stays ahead of the competition. Barco Silex' history as a custom electronic design house (ASIC, FPGA, DSP, Board) specialized in video coding, cryptography, security and memory controllers goes back to 1991, offering the best guarantee for continuous support throughout the complete lifecycle of products.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order reference: **BA110**

A board-based demo setup and evaluation kit is available and can be ordered separately as an option. Cryptography cores (AES) are also available and can be ordered separately.

For additional information and other IP products contact:

Barco – Silex

e-mail: barco-silex@barco.com

<http://www.barco.com/jpeg2000>

<http://www.barcodesignservices.com>

or the local Barco Silex design centers:

Belgium

Scientific Park
Rue du Bosquet 7
1348 Louvain-la Neuve
+32(0)10/45.49.04

France

ZI Peynier- Rousset
Route de Trets - Imm CCE
13790 Peynier
+33(0)44/216.41.06