

# JPEG color encoder

BA116JPEGCE Factsheet

## Features

- High-speed sustained single clock cycle per pixel component encoding
- Single clock cycle Huffman encoding
- 100 % baseline ISO/IEC 10918-1 JPEG compliance for colour images (single- and multi-scan formats) extending to effective 255-scan support
- Full header building capability and automatic internal Huffman and quantization tables programming based on header data
- Full JPEG format and abbreviated format support, including restart markers and restart interval
- One-pass encoding scheme with bit rate regulation if enabled
- Simple FIFO interfaces for compressed data (32 bits) and pixel interfaces (8 bits)
- Simple CPU interface for encoder and headers programming
- Easy-to-use status and control interface
- Programmable external interrupt for event follow-up
- Four entropy tables (two DC, two AC), four quantization tables
- Burst image-sequence encoding support for images with identical tables
- 8 bits/pixel component
- 8x8 block-format pixel input with classical scan order (row by row from left to right)
- Fully synchronous hardware design
- Fully stallable compressed-data and pixel interfaces
- Throughputs ranging from sub CIF 25Hz to SDTV to HDTV1280x720 50Hz

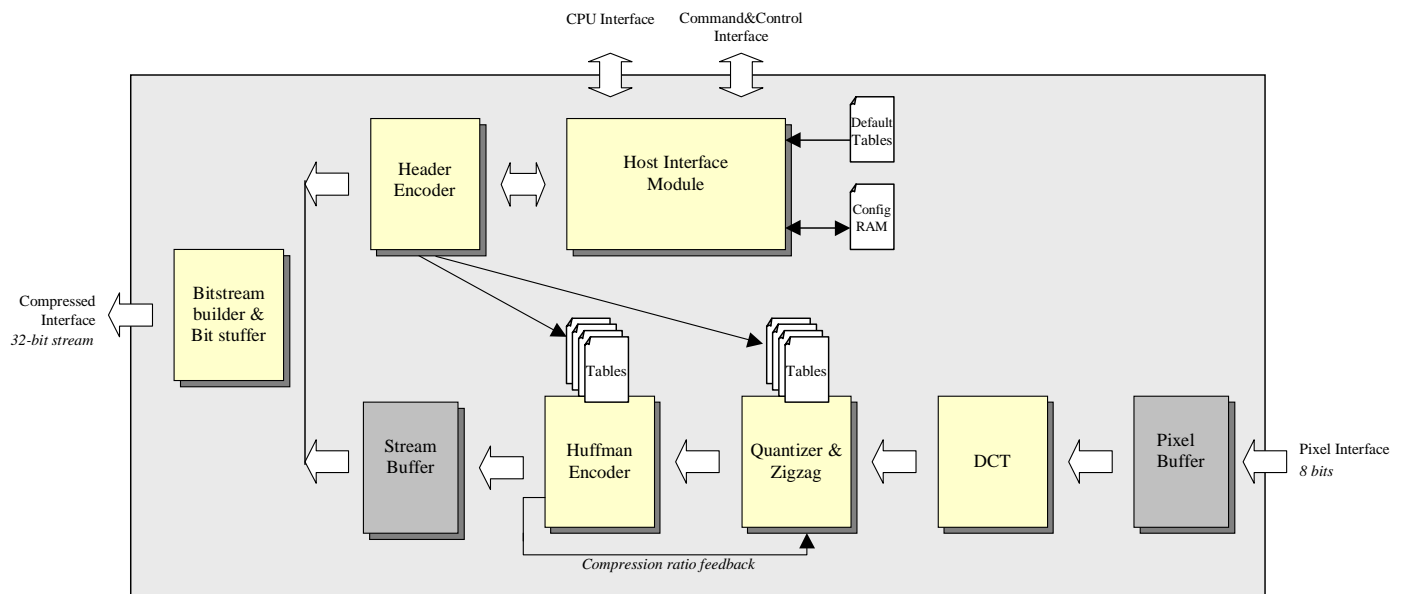


Figure 1

**Barco-Silex**  
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## General description

The JPEG core is intended for high-speed encoding of gray-scale, colour or multi-scan images coded with ISO/IEC 10918-1 baseline coding standard. The encoder supports all features of the baseline standard, including restart markers, DNL, user-definable comments and application markers. It is able to encode abbreviated-format or full-format images, with pre-defined default entropy and quantization tables if preferred.

Its autonomous behaviour, its simple FIFO-like interfaces and its 100% synchronous structure allow to integrate it very easily in a complex system with few effort. This is reinforced by the stand-alone ability of the encoder that allows to instantiate it in systems with few CPU intervention.

## Applications

The encoder is suitable for applications involving baseline-DCT JPEG compression in a gray-level, colour or multi-scan environment. Applications requiring high pixel through-put can be addressed by the core. These include printers, scanners, digital cameras, medical imaging, archiving...

## Implementation data

Device	Logic	# of Clk	Performance (MHz)	Needed Resource
Altera EP1S25F1020C7	8850 LE	1	58	18 M4K, 5 DSP Multipliers
Xilinx XC2V1000-4	4379 slices	1	76	11 RAMB, 2 MULT
Xilinx XC3S1000-4	4388 slices	1	54	11 RAMB, 2 MULT
UMC 0.18 $\mu$ m	64 kgates	1	142	36.5 kbits

## Pinout description

Name	I/O	Comments
<b>Pixel interface</b>		
PIXEL[7:0]	I	Block-scan ordered pixels
nEOIout	O	End of image
nEOSout	O	End of current scan
nEOBout	O	End of current block
nWait	I	Pixel stalling request
nStop	I	Block stalling request
nPixWen	I	Pixel strobe (active low)
nLastPixOI	I	Last pixel of image (for DNL support with single scan)
nLastPixOS	I	Last pixel of image (for DNL support with multi-scan)
<b>Command interface</b>		
nReset	I	Asynchronous reset
GO	I	"Start encoding" command
LastPict	I	End of image burst
LastScan	I	End of scan burst
nEndI	O	End of image encoding process
nEndS	O	End of scan encoding process
CLK	I	Clock
<b>Compressed data interface</b>		
CODE [31:0]	O	Compressed data
nWrEn	O	Synchronous FIFO write command (active low)
WrEn	O	Synchronous FIFO write command (active high)
nFF_IR	I	Synchronous FIFO full flag for compressed data
nWrEn_nOE	O	nWrEn/WrEn output enable
nJpegEn	I	Compressed data interface stalling command
<b>CPU interface</b>		
XD [7:0]	I/O	CPU data bus
DataOE	O	XD output enable
XA [10:0]	I	CPU address bus
WrRdIn	I	CPU transfer direction
nCS	I	CPU chip select
nINT	O	Interrupt

\* '#' takes value from 0 to n-1 where n is the number of entropy channels implemented in parallel.

## Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

- image processing
- communications
- consumer electronics
- industrial electronics.

## Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

## More information

Order-reference: **BA116JPEGCE**

For additional information and other IP products contact:

Barco – Silex

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