

JPEG grayscale decoder

BA117JPEGGD Factsheet

Features

- High-speed sustained single clock cycle per pixel decoding
- Single clock cycle Huffman decoding
- 100 % baseline ISO/IEC 10918-1 JPEG compliance for gray-scale images (single scan format)
- Full header parsing capability and automatic on-the-fly Huffman and quantization tables reprogramming from header data
- Header error catching features
- Full JPEG format and abbreviated format support, including restart markers
- Simple FIFO interfaces for compressed data (32 bits) and pixel interfaces (8 bits)
- Simple CPU interface for decoder programming
- Easy-to-use status and control interface through seven internal registers
- Programmable external interrupt for event follow-up
- Two entropy tables (one DC, one AC), one quantization table
- Burst image-sequence decoding support for images with identical tables
- 8 bits/pixel
- 8x8 block-format pixel output with classical scan order (row by row from left to right)
- Fully synchronous hardware design
- Fully stallable compressed-data interface; stallable pixel interface on a block-by-block basis
- IEEE 1180-1990 compatible IDCT for number precision requirements

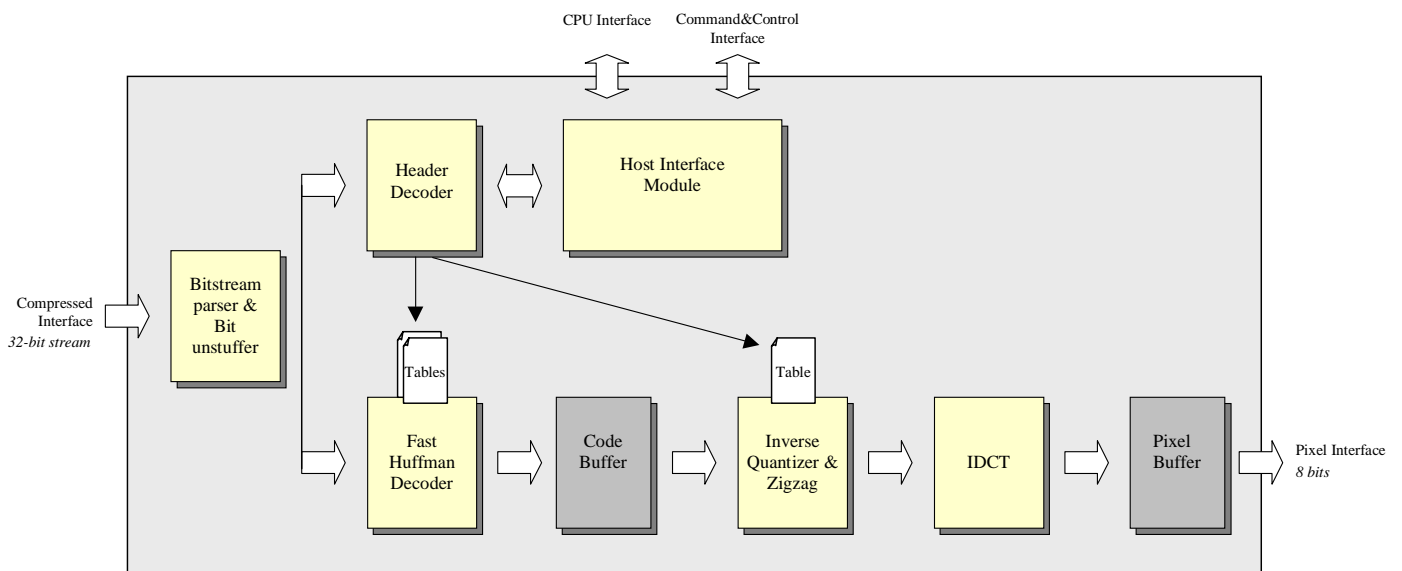


Figure 1

General description

The JPEG core is intended for high-speed decoding of gray-scale images coded with ISO/IEC 10918-1 baseline coding standard. The decoder supports all features of the baseline standard, including restart markers and full header parsing. It is able to decode abbreviated-format or full-format images, automatically extracting the quantization and entropy tables.

Its autonomous behaviour, its simple FIFO-like interfaces and its 100% synchronous structure allow to integrate it very easily in a complex system with few effort. This is reinforced by the stand-alone ability of the decoder that allows to instantiate it in systems without CPU intervention.

Applications

The decoder is suitable for applications involving baseline-DCT JPEG decompression in a gray-level environment. Applications requiring high pixel through-put can be addressed by the core. These include printers, scanners, digital cameras, medical imaging, archiving,...

Implementation data

Device	Logic	# of CLK	Performance (MHz)	Needed Resource
Altera EP20K400CBC652C7	9816 LE	1	57	66 ESB
Altera EP2A15F672C7	9797 LE	1	69	44 ESB
Xilinx XC2V1000-4	3459 Slices	1	73	15 Block RAMs
Xilinx XCV300E-8	3039 Slices	1	64	14 Block RAMs
Xilinx XCV300-6	3039 Slices	1	48	14 Block RAMs

Pinout description

Name	I/O	Comments
Decoder pixel interface		
PIXEL[7:0]	O	Block-scan ordered decoded pixels
DSYNC_N	O	Start-of-block sync signal
JETEOI_N	O	End of image
STOP_N	I	Pixel stalling request
PIXWEN_N	O	Pixel strobe (active low)
PIXWEN	O	Pixel strobe (active high)
Command interface		
JETRST_N	I	Asynchronous reset
JETEND_N	O	End of decoding process
GO_N	I	"Start decoding" command
LASTPICT_N	I	End of image burst
CLK	I	Clock
Compressed data interface		
CODE [31:0]	I	Compressed data
FFCREN_N	O	Synchronous FIFO read command (active low) for compressed data
FFCREN	O	Synchronous FIFO read command (active high) for compressed data
FFCEF_N	I	Synchronous FIFO empty flag for compressed data
FTMFIFO	I	FIFO type: classical or fall-through-mode
JPGEN_N	I	Compressed data interface stalling command
CPU interface		
XD [7:0]	I/O	CPU data bus
XA [3:0]	I	CPU address bus
WRRD_N	I	CPU transfer direction
JETCS_N	I	CPU chip select
JETINT_N	O	Interrupt

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- image processing
- communications
- consumer electronics
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- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order-reference: **BA117JPEGGD**

For additional information and other IP products contact:

Barco – Silex

e-mail: barco-silex@barco.com

<http://www.barcodesignservices.com>

or the local Barco Silex design centers:

Belgium	France
Scientific Park	ZI Peynier- Rousset
Rue du Bosquet 7	Route de Trets Imm CCE
1348 Louvain-la Neuve	13790 Peynier
+32(0)10/45.49.04	+33(0)44/216.41.06