Features

- **Sub-frame latency decoding (< 5ms)**
- **Full image decoding (no tiling)**
- Compliant with JPEG 2000 (ISO/IEC 15444-1)
- Integrated Intellectual Property (IP) core for JPEG 2000
- Single-chip FPGA solution:
  - HD: 720p30-180, 1080i30-180, 1080p30-90
  - DCI: 2K, 4K
  - Custom frame sizes up to 8K or larger
- Customizable input bit rate: up to 200Mbps / 400Mbps
- YUV 4:2:2 color space
- Supported JPEG 2000 parameters:
  - Pixel depth: up to 12 bits per color sample
  - Full-frame decoding (no tiling)
- Fully autonomous decoder with automatic parameter extraction, minimal user intervention
- Fully synchronous design
- Can be used for FPGA, ASIC and Structured ASIC technologies
- Can be integrated with Barco Silex cryptography cores for advanced stream protection

![Diagram](image_url)
General description

Capitalizing on its long-term experience with JPEG 2000 hardware coding, Barco Silex offers a large JPEG 2000 portfolio including this compact, real-time hardware decoder engine that is optimized for low latency video applications. The core architecture offers a flexible and high-speed solution to meet the challenges of high-end broadcast performance requirements, sustaining up to 180 frames per second in 1080i format, for compressed stream bitrates extending up to 400 megabit per second.

The BA129 core decodes streams that are compliant with the ISO/IEC 15444-1 specification (JPEG 2000) and supports single-tiled frames up to 1080p or larger. This IP is the complement of the BA130 low-latency JPEG 2000 encoder IP, to which it can be directly connected.

The core performs the complete video decompression operations of the normalized decoding process: stream parsing and header decoding, entropy decoding, inverse quantization and inverse discrete wavelet transform (IDWT). It accepts a JPEG 2000 file at its input interface and generates decoded samples at its output interface with up to 12 bits per color sample, an optional module generates the video output in real-time, without any buffering, to preserve the latency performances.

The BA129 IP provides a single-chip FPGA solution for 720p30-180, 1080i30-180 and 1080p30-90 video modes, with a total pixel-to-pixel latency below 9ms for 1080i/p60, below 5ms for 1080i/p120 and below 3ms for 1080i/p180 when used together with the BA130 encoder.

The flexible FPGA architecture allows the user to build a secure decoder by integrating Barco Silex cryptography IP cores.

Applications

- Digital video broadcasting, contribution, ...
- Camera equipments
- Remote control
- Wireless video

The BA129 JPEG 2000 decoder can also be integrated in a variety of other applications with similar high-demanding processing requirements. The underlying architecture of the core allows for a wide range of features and performance options, as well as specific customizations.
Technical description

Figure 1 illustrates a simplified block diagram of the BA129 IP showing the internal modules and the interfaces. The IP core features 4 main interfaces: a stream interface, a pixel interface, a control interface and a memory interface for intermediate large data storage and stream parsing. The decoder control interface allows the user to trigger decoding and to monitor the status of the decoding process.

The decoder requires a single external memory to store the intermediate buffered data. The core implements these memory channels as a generic multi-port interface to a memory controller. This will typically be a DDR2/DDR3 SDRAM controller.

The memory requirements for the IP are as follows:

<table>
<thead>
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<th>Version</th>
<th>SDRAM size</th>
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<tr>
<td>HD (1920x1080)</td>
<td>32 MB</td>
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</table>

The following sections describe the modules constituting the BA129 core as depicted under Figure 1.

JPEG 2000 stream parser
This module analyses the headers, unpacks the compressed data and sends them to the entropy decoding unit.

Entropy decoder (modeler and arithmetic decoder)
This module gets compressed coding passes from the parser and converts them to quantized code blocks. The Modeler gives the sequencing of the entropy decoding: it reconstructs the code block bitplane by bitplane from the most significant to the least significant and places relevant bits in zigzag order in each bit plane. Moreover it computes the context information needed by the arithmetic decoder. The contexts and the bit stream provided by the parser are processed by the Arithmetic Decoder that generates the decoded bits placed at the appropriate location by the Modeler.

Frame assembler
This unit reconstructs subbands based on the codeblocks coming from the entropy decoder. It outputs decoded codeblocks into the external memory at the corresponding location inside the subband they belong to.

Inverse quantizer
The inverse quantizer applies an inverse quantization step as specified in the stream header. A different inverse quantization step is available for each subband resulting in differently weighted frequency subbands. The quantization steps are extracted from the JPEG 2000 file headers by the header parser.

2D IDWT
This module performs the inverse 2D wavelet transform. It is able to process frames without tiling. It performs wavelet re-composition on the subbands situated in the off-chip buffer with a programmable number of decomposition levels as specified in the stream header. The wavelet engine stores its temporary results in the external memory.

Host interface
This interface provides status and command interfaces at the disposal of the user. These are used to trigger decoding of JPEG 2000 files and to follow the status of the decoding process. User intervention is minimized as the core has a completely autonomous behavior.

Memory controller
The JPEG 2000 decoding core uses external memory to store temporary intermediate data to ensure smooth and efficient processing of the video stream. This is usually achieved by using DDR2/DDR3 SDRAM. The JPEG 2000 decoder IP core interfaces with the memory controller through an easy generic multi-port interface to adapt the decoding architecture to the exact board topology.
Implementation technologies

The BA129 JPEG 2000 decoder is compact and fast, providing the high level of performances required for HD video. It is also flexible and portable to support different FPGA families and ASIC technologies. We commit to continuously keeping our cores at a state-of-the-art optimization level for the newest FPGA devices on the market. We offer solutions for Xilinx Virtex-5, Virtex-6, Spartan-6 and Altera Stratix-3, Stratix-4, Arria-2GX, Cyclone-3 and Cyclone-4 devices.

Please contact us for detailed implementation data.

Barco Silex overview

Barco Silex is a leader in contract engineering services, custom hardware and software development, as well as Intellectual Property (IP). Its high quality JPEG 2000 IP cores, developed since 2002, are optimized for all leading-edge FPGAs as well as for legacy platforms.

Thanks to its continued stream of aggressive innovations, Barco Silex stays ahead of the competition. Barco Silex’ history as a custom electronic design house (ASIC, FPGA, DSP, Board) specialized in video coding, cryptography, security and memory controllers goes back to 1991, offering the best guarantee for continuous support throughout the complete lifecycle of products.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions. All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:
- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGA's or ASIC's, while meeting short time to market constraints.

More information

Order reference: BA129

A board-based demo setup and evaluation kit is available and can be ordered separately as an option. Cryptography cores are also available and can be ordered separately.

For additional information and other IP products contact:
Barco – Silex
e-mail: barco-silex@barco.com
http://www.barco.com/jpeg2000
http://www.barcodesignservices.com

or the local Barco Silex design centers:

<table>
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</tr>
<tr>
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<td>Route de Trets - Imm CCE</td>
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Technical specifications are subject to change without prior notice