

JPEG 2000 Encoder Sub-frame latency

BA130 - Factsheet

Features

- **Sub-frame latency encoding (< 6ms)**
- **Full image encoding (no tiling)**
- **Compliant with JPEG 2000 (ISO/IEC 15444-1)**
- Integrated Intellectual Property (IP) core for JPEG 2000
- Single-FPGA solution:
 - HD: 720p30-180, 1080i30-180, 1080p30-90
 - DCI: 2K, 4K
 - Custom frame sizes up to 8K or larger
- Customizable output bit rate: up to 200Mbps / 400Mbps
- YUV 4:2:2 color space
- Supported JPEG 2000 parameters:
 - Pixel depth: up to 12 bits per color sample
 - Full frame encoding (no tiling)
 - Flexible Tier-2 for rate allocation
 - Quality: quantization, weights, ...
- Minimal user intervention
- Fully synchronous design
- Can be used for FPGA, ASIC and Structured ASIC technologies
- Can be integrated with Barco Silex cryptography cores for advanced stream protection

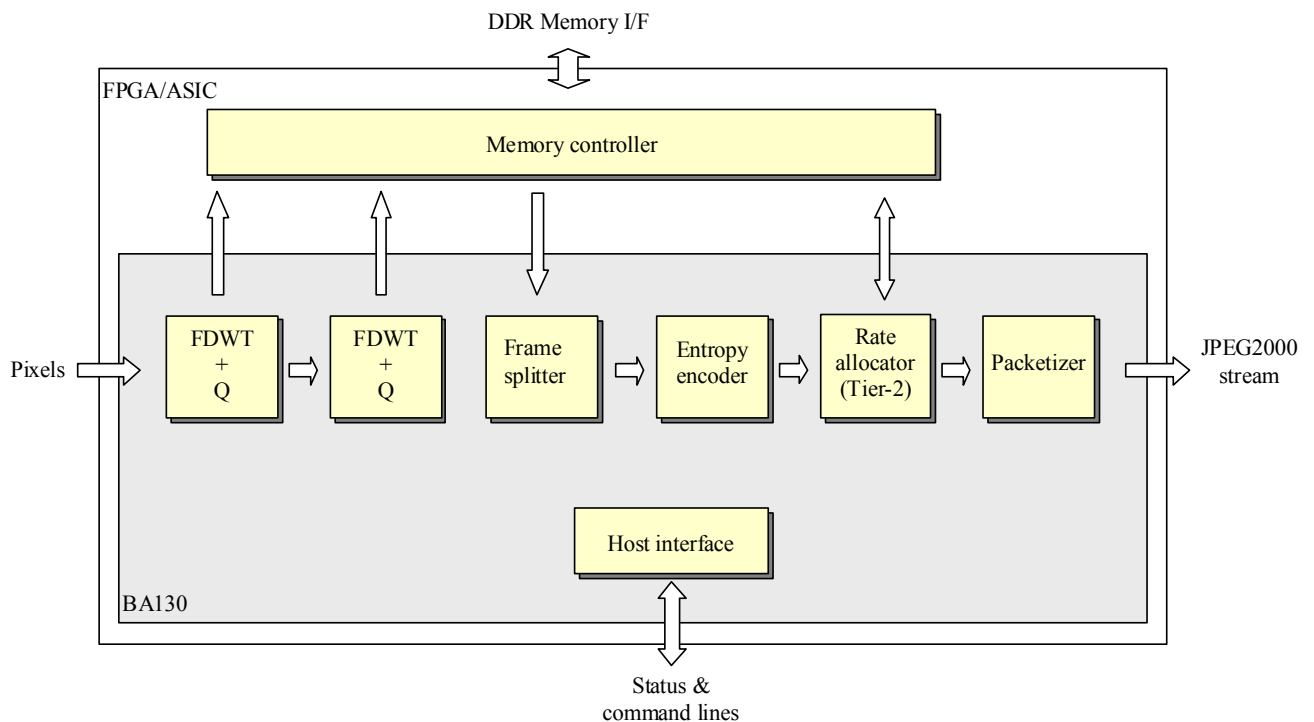


Figure1

Version: 1.4

www.barco.com/jpeg2000
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General description

Capitalizing on its long-term experience with JPEG 2000 hardware coding, Barco Silex offers a large JPEG 2000 portfolio including this compact real-time hardware encoder engine that is optimized for low-latency video applications. The core architecture offers a flexible and high-speed solution to meet the challenges of high-end broadcast applications. The BA130 is able to sustain up to 180 frames per second in 1080i format, for compressed stream bitrates extending up to 400 megabit per second.

The BA130 IP core encodes YUV 4:2:2 frames up to 1080p or larger and generates compressed stream which are compliant with the ISO/IEC 15444-1 specifications (JPEG 2000).

The BA130 IP is the complement of the BA129 sub-frame latency JPEG2000 decoder IP, to which it can be directly connected.

The IP core performs the complete video compression operations of the normalized encoding process:

- Discrete wavelet transform (DWT)
- Quantization
- Entropy encoding
- Rate allocation
- Stream packetizing

The BA130 accepts pixels on its input interface with up to 12 bits per color components and it generates a JPEG 2000 compliant stream. Optional modules can be provided for video interfacing and temporary output stream buffering in order to facilitate the integration process.

The BA130 IP provides a single-FPGA solution for 720p30-180, 1080i30-180 and 1080p30-90 video modes, with a total pixel-to-pixel latency below 9ms for 1080i/p60, below 5ms for 1080i/p120 and below 3ms for 1080i/p180 when used together with the BA129 decoder.

The flexible FPGA architecture allows the user to build a secure encoder by integrating Barco Silex cryptography IP cores.

Applications

- Digital video broadcasting, contribution, ...
- Camera equipments
- Remote control
- Wireless video

The BA130 sub-frame latency JPEG 2000 encoder can also be integrated in a variety of other applications with similar high-demanding processing requirements. The underlying architecture of the core enables a wide range of features and performance options, as well as specific customizations.

Technical description

Figure 1 illustrates a simplified block diagram of the BA130 IP showing the internal modules and the interfaces. The IP core features 4 main interfaces: a pixel interface, a stream interface, a control interface and a memory interface for intermediate large data storage. The encoder control interface allows the user to parameter the core, trigger encoding and monitor the status of the encoding process.

The encoder requires a single external memory containing intermediate buffered data. The core implements these memory channels as a generic multi-port interface to a memory controller. This will typically be a DDR2/DDR3 SDRAM controller.

The memory requirements for the IP are as follows:

Version	SDRAM size
HD (1920x1080)	64 MB

The following sections describe the modules constituting the BA130 core as depicted under Figure 1.

2D FDWT

This module performs the forward 2D wavelet transform. It is able to process frames without tiling. It performs wavelet decomposition with a programmable number of decomposition levels as specified by the user. The wavelet engine stores its temporary results in the external memory.

Quantizer

The quantizer applies quantization steps as specified by the user. Specific quantization step is programmable for each subband resulting in differently weighted frequency subbands.

This module also divides the decomposed subbands into code blocks and dispatches the various code blocks to the entropy encoding channels. This is done by reading the code blocks from the external memory at the appropriate location inside the subband they belong to.

Entropy encoder (modeler and arithmetic encoder)

This module generates compressed coding passes (JPEG 2000 codestream) from the quantized code blocks it receives from the quantizer. The Modeler gives the sequencing of the entropy encoding: it decomposes the code block bitplane by bitplane from the most significant to the least significant and places relevant bits in zigzag order in each bit plane. Moreover, it computes the context information needed by the arithmetic encoder. The contexts and binarized code blocks are processed by the Arithmetic Encoder that generates the bitstream which is ready to be encapsulated in a JPEG 2000 file.

Rate allocator

This module performs optimal rate allocation based on the metrics information produced by the entropy encoder, for the purpose of constraining the generated bit rate. This module also embeds the generated codestream in a JPEG 2000 file container ready for decoding by any JPEG 2000 compliant decoder.

The rate allocator is configured by the user to target one of the 3 supported rate-control modes: constant quality, constant bit rate, constant quality with maximum bitrate. The user can select the rate-control mode on a frame-by-frame basis.

Packetizer

The packetizer generates the main header, the tile-part header and tag trees combined with the compressed bitstream to produce a complete, ISO/IEC 15444-1-compliant output stream.

Host interface

This interface provides configuration, status and command interfaces at the disposal of the user. It is used to parameterize the JPEG 2000 process, trigger encoding and to follow the status of the encoding process. User intervention is minimized.

Memory controller

The JPEG 2000 encoding core uses external memory to store temporary intermediate data to ensure smooth and efficient processing of the video stream. This is usually achieved by using DDR2/DDR3

SDRAM. The JPEG 2000 encoder IP core interfaces with the memory controller through an easy generic multi-port interface allowing the user to adapt the encoding architecture to the exact board topology.

Implementation technologies

The BA130 JPEG 2000 encoder is compact and fast, reaching speeds suitable for high-end HD video applications. It is also flexible and portable to support different FPGA families and ASIC technologies. We commit to continuously keep our cores at a state-of-the-art optimization level for the newest FPGA devices on the market. We offer solutions for Xilinx Virtex-5, Virtex-6, Spartan-6 and Altera Stratix-3, Stratix-4, Arria-2GX, Cyclone-3 and Cyclone-4 devices.

Please contact us for detailed implementation data.

Barco Silex overview

Barco Silex is a leader in contract engineering services, custom hardware and software development, as well as Intellectual Property (IP). Its high quality JPEG 2000 IP cores, developed since 2002, are optimized for all leading-edge FPGAs as well as for legacy platforms.

Thanks to its continued stream of aggressive innovations, Barco Silex stays ahead of the competition. Barco Silex' history as a custom electronic design house (ASIC, FPGA, DSP, Board) specialized in video coding, cryptography, security and memory controllers goes back to 1991, offering the best guarantee for continuous support throughout the complete lifecycle of products.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions. All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off-the-shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGA's or ASIC's, while meeting short time to market constraints.

More information

Order reference: **BA130**

A board-based demo setup and evaluation kit is available and can be ordered separately as an option. Cryptography cores are also available and can be ordered separately.

For additional information and other IP products contact:

Barco – Silex

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