

MPEG-4 Simple Profile Encoder

BA131MPEG4E Factsheet

Features

- Compliant with ISO/IEC 14496-2: Information technology – Coding of audio-visual objects – Part 2: Visual
- Support for Simple Profile with resolution user definable up to 4CIF (incl. levels L1 to L5)
- Real-time 4CIF encoding at 30 frames per second
- Support for I-VOP and P-VOP, with configurable interval between successive I-VOPs
- Advanced motion estimation (directional search), with automatic Intra macroblock detection
- +15/-16 motion search window
- Half-pixel motion precision
- Single motion vector per macroblock
- Power savings mechanisms
- AC/DC coefficient prediction
- Constant Bit Rate option available through Microblaze or Nios code with advanced bit rate regulation algorithm, using statistical information available from the motion estimation engine
- Easy synchronous pixel and stream interfaces
- Easy control and status interface through simple CPU interface
- Off-chip reference frame store, with easy memory interface pluggable to any custom memory controller (SRAM or SDRAM for instance)
- Minimized off-chip data bandwidth
- Full header processing
- Optional support for multiple simultaneous streams encoding
- Optimized for Stratix, StratixII, CycloneII, Virtex2, Virtex2PRO, Spartan3, Spartan3E and Virtex4 FPGA's

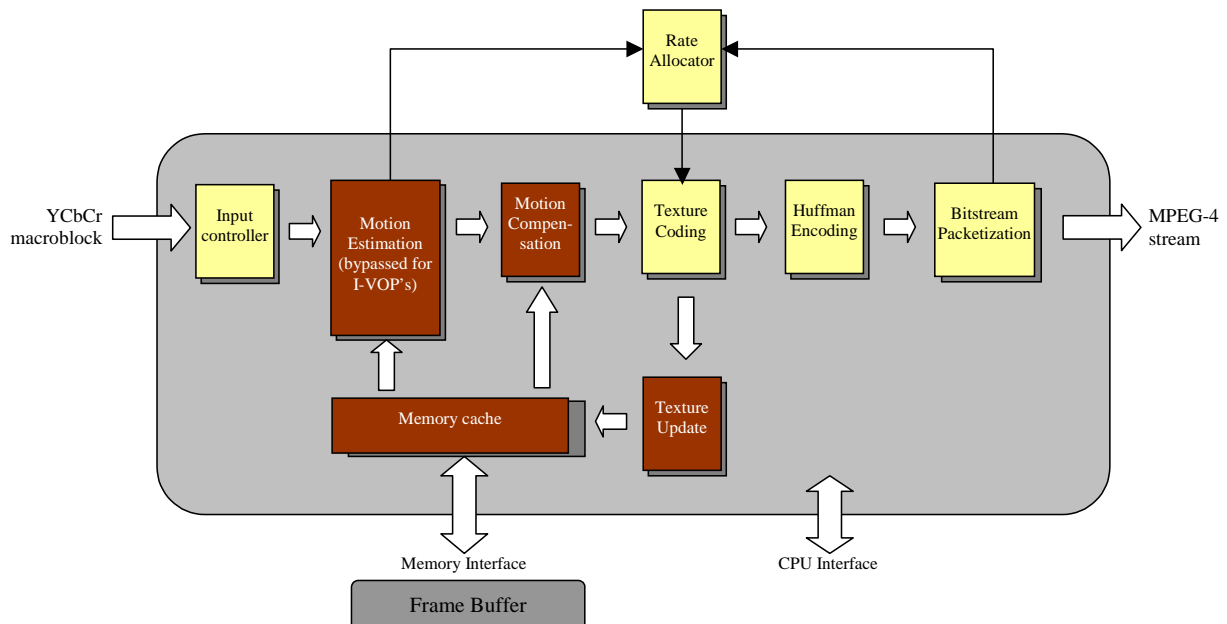


Figure 1: Block diagram

General description

The MPEG-4 encoder is a hardware module optimized for FPGA technologies, making use of a limited number of logic resources and being able to encode a 4CIF (704x576) sequence in real time.

It is fully compliant with the Video part of ISO/IEC 14496-2. All visual tools of the Simple Profile are implemented, including full support of I-VOP (intra-coded frames, without motion estimation) and P-VOP (predictive-coded frame, with motion estimation on previously encoded frame). The core is a good compromise between coding efficiency (resulting in lower bit rate for same quality), logic complexity and coding throughput, thanks to the use of an efficient motion estimation algorithm (directional search) leading to fast and precise matching, at half pixel resolution, of blocks between the current frame and its reference.

Supported image resolutions include pre-defined levels Level1 to Level5(QCIF/CIF/VGA/SDTV) and custom definitions up to 4CIF (704x576). The core can be customized to provide support for even larger resolutions, such as HD format.

The core features a Variable Bit Rate mode (VBR mode: fixed, user-specified quality). It can optionally also provide Constant Bit Rates (CBR mode: with regulation of the output bit rate) by using an external small microprocessor running a rate allocation algorithm (such as Nios or Microblaze). When used in CBR mode, the core delivers high-quality regulation thanks to its patented rate allocation algorithm making use of statistical information available at the motion estimation engine.

Applications

- Video broadcast
- Security and Surveillance
- Multimedia streaming over TCP/IP
- Mobile communications

Technical description

Figure 1 illustrates a simplified block diagram of the BA131MPEG4E IP showing the internal modules and its interfaces.

The video data is organized in macroblocks under YUV format (4:2:0 resolution). One macroblock is made of 4 luminance blocks (8x8), 1 Cb block (8x8) and 1 Cr block (8x8). The video data is sent to the core through its video interface in macroblock raster scan order. It generates the compressed stream at its Compressed Data Interface. The stream contains fully compliant headers and is regulated to a given bit rate if the CBR option is enabled (together with external microprocessor running the rate allocation algorithm).

The encoder has a generic interface to a memory controller, allowing the connection to any custom memory controller. Thanks to the burst nature of data transfers at this interface, the core can be used with simple SRAM but also SDRAM or DDR SDRAM. The core can be delivered with a standard SRAM controller; a suitable SDRAM controller is separately available. The core has been optimized in order to minimize the amount and bandwidth of off-chip memory. A single frame needs to be stored and accesses are reduced to 1 read and 1 write per input sample.

The encoder has a simple generic interface to an external CPU in order to configure the various parameters of the core and to monitor the status of the encoding process.

The following sections describe the modules constituting the BA131MPEG4E core as depicted under Figure 1.

Motion estimation

The first module of the core is the motion estimation engine. This module is bypassed for Intra-coded pictures (I-VOP), which are not coded with reference to any other picture.

The motion estimation engine uses an advanced directional search algorithm able to precisely and rapidly match the current macroblock (16x16 pixels) with its equivalent in the reference frame. The core uses the frame stored in external memory as a reference. The processing generates one motion vector per macroblock, giving the direction and amplitude of the detected motion. The matching precision is half a pixel.

The motion estimation engine features advanced capabilities in order to shorten the search time as much as possible. This module also delivers statistics used by the rate allocation algorithm. The module also detects when a macroblock cannot be registered correctly to the reference frame and should better be encoded as an Intra macroblock.

Motion compensation

This module computes the estimation error induced by the use of the vector generated by the motion estimation engine. This module is bypassed for Intra-coded pictures (I-VOP). It makes the difference between the current macroblock (in luminance and chrominance planes) and the predicted macroblock from the reference frame, using the estimated motion vector. The result is known as the prediction error and must be encoded by the texture coding.

Texture coding

This module encodes error frames when using P-VOPs (resulting from motion compensation) or complete frames when using I-VOPs. This module has advanced low-power features where part of the processing is switched off when it is detected to be useless. An approximation of its result is then used instead.

The texture coding is made of Discrete Cosine Transform (DCT), AC/DC prediction, quantization and zigzag encoding and works on block level (8x8):

- The DCT decorrelates the frequency contents of the 8x8 blocks and delivers a matrix of 64 frequency coefficients, representing the frequency contents of the original block of data.
- This is then quantized using a scalar quantizer. The quantization factor is programmable by the user, allowing him to set the quality level.
- The AC/DC predictor is used for I-VOPs and performs a prediction of the first line or the first column of the quantized matrix, based on the transformed blocks situated on the left and on top of the current block. The prediction source (top or left) is determined by a gradient analysis of DC coefficients of the transformed blocks situated on top, top-left and left. This prediction results in a higher compression efficiency.
- The quantized matrix is then processed by the zigzag encoder, which reads this 8x8 matrix in a pre-defined scan order; this results in a chain of coefficients where most of these are zero's. This is then further encoded thanks to a run encoder in order to reduce the size of the representation.

Entropy encoder

The entropy encoder finalizes the data compression by applying a Huffman encoding to both the motion vectors and the compressed pixels. This module uses pre-defined look-up tables.

Bitstream packetization

This module generates compliant MPEG-4 VOL and VOP headers (short headers and data partitioning are not supported but the core can be customized to add these features).

The encoder includes an output buffer allowing the user to generate a stream at constant bit rate (CBR mode) by coupling the core to a small microprocessor running a rate allocation algorithm (Nios or Microblaze for instance). The rate allocation algorithm can be purchased optionally.

Texture update

This feedback loop is performing the inverse operations of the texture coding: unzigzag, inverse quantization and Inverse Discrete Cosine Transform (IDCT). This allows the encoder to take into account quantization errors occurring at the decoder side when the picture is decoded. The encoder then uses the result of this texture update module to update the contents of the frame store (when needed). This new contents is then ready to be used as a reference frame for encoding the next frame.

Rate allocator

This optional module is dedicated to regulate the output of the encoding IP core to the bit rate specified by the user. This module makes use of a patented rate allocation algorithm, exploiting statistical information available at the motion estimation to improve its efficiency and provide a more stable stream bit rate and quality.

This module is implemented as software code able to run on a simple processor (Nios or Microblaze for instance). The rate allocator can also be customized to be mapped as a 100% hardware block.

Implementation data

The following table details implementation results of the BA131MPEG4E core on various FPGA technologies. The core is 100% RTL and ASIC technologies can also be mapped. Performance figures enable real-time encoding for all Simple Profile L1 to L5 levels.

Device	Logic	# of Clk	Performance (MHz)	Needed Resource	Troughput (Msamples/s) ¹⁾
Altera EP1S25C5 ²⁾	18000 LE's	1	100	92 M4K, 16 DSP Multipliers	18.2
Xilinx XC2V2000-4	9000 Slices	1	100	30 RAMB16, 16 MULT18x18	18.2

1) Results for typical compression, as measured on difficult video sequences

2) Estimated (contact us for latest figures)

Pinout description

Name	I/O	Size	Comments
Global			
CLK	I	1	Clock
RESET	I	1	Global asynchronous reset
CPU Interface			
XENA	I	1	Chip Select
XWEA	I	1	Access direction
XADDR	I	5	Address lines
XQ	O	32	Read data
XD	I	32	To-be-written data
Pixel Interface			
PEMPTY	I	1	Pixel not ready
PQ	I	8	Pixel data
PRE	O	1	Pixel read enable
Compressed Data Interface			
CWE	O	1	Compressed data strobe
CDATA	O	8	Compressed data
CFULL	I	1	Compressed data not ready flag
Memory Interface (read queue)			
MRQFULL	I	1	Read request queue full
MRQPUSH	O	1	Push read request
MRQADDR	O	32	Read request address
MRQEMPTY	I	1	Read data queue empty
MRQPOP	O	1	Pop read data
MRQRD	I	32	Read data (16-word burst)
Memory Interface (write queue)			
MWQFULL	I	1	Write request queue full
MWQPUSH	O	1	Push write request
MWQADWD	O	32	Write request address and write data (16-word burst)

Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

- image processing
- communications
- consumer electronics
- industrial electronics.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order-reference: **BA131MPEG4E**

For additional information and other IP products contact:

Barco – Silex

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