

MPEG-4 Simple Profile Decoder

BA132MPEG4D Factsheet

Features

- Compliant with ISO/IEC 14496-2: Information technology – Coding of audio-visual objects – Part 2: Visual
- Support for Simple Profile with resolution user definable up to 4CIF (incl. levels L1 to L5)
- Real-time 4CIF decoding at 30 frames per second
- Support for I-VOP and P-VOP
- Motion compensation with +15/-16 motion window
- Half-pixel motion precision
- Single motion vector per macroblock (4MV not supported)
- AC/DC coefficient prediction
- Easy synchronous pixel and stream interfaces
- Off-chip reference frame store, with easy memory interface pluggable to any custom memory controller (SRAM or SDRAM for instance)
- Minimized off-chip data bandwidth
- Full header decoding (data partitioning and short headers not supported)
- Reversible VLC decoding not supported
- Simultaneous multiple streams decoding
- Optional support for multiple simultaneous streams decoding
- Optimized for Stratix, StratixII, CycloneII, Virtex2, Virtex2PRO, Spartan3, Spartan3E and Virtex4 FPGA's

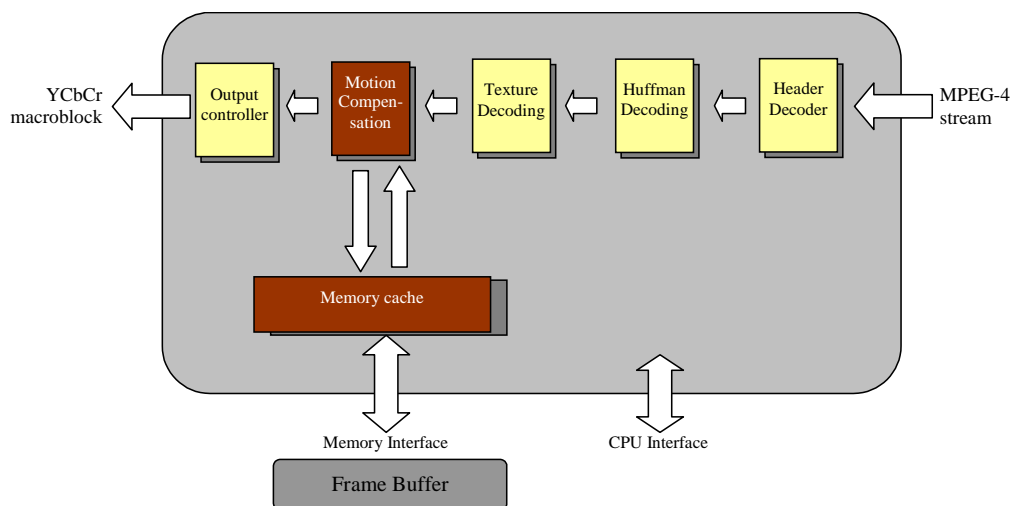


Figure 1: Block diagram

General description

The MPEG-4 decoder is a hardware module optimized for FPGA technologies, making use of a limited number of logic resources and being able to decode a 4CIF (704x576) sequence in real time. The decoder can also be used to decode multiple streams simultaneously (up to 8).

It is compliant with the Video part of ISO/IEC 14496-2. Most of the visual tools of the Simple Profile are implemented, including support of I-VOP (intra-coded frames, without motion estimation) and P-VOP (predictive-coded frame, with motion estimation on previously encoded frame).

The following tools are supported:

- Half pixel motion
- I-VOP, P-VOP

The following tools are not supported:

- 4MV
- Error resilience (data partitioning, reversible VLC decoding and slice resynchronization)
- Short header (on demand the core can be customized to support this)

Supported image resolutions include pre-defined levels Level1 to Level5 (QCIF/CIF/VGA/SDTV) and custom definitions up to 4CIF (704x576). The core can be customized to provide support for even larger resolutions, such as HD format.

Applications

- Video broadcast
- Security and Surveillance
- Multimedia streaming over TCP/IP
- Mobile communications

Technical description

Figure 1 illustrates a simplified block diagram of the BA132MPEG4D IP showing the internal modules and its interfaces.

The core accepts the compressed stream at its Compressed Data Interface. The stream contains headers. The decoded video data is organized in macroblocks under YUV format (4:2:0 resolution). One macroblock is made of 4 luminance blocks (8x8), 1 Cb block (8x8) and 1 Cr block (8x8). The video data is output by the core through its video interface in macroblock raster scan order.

The decoder has a generic interface to a memory controller, allowing the connection to any custom memory controller. Thanks to the burst nature of data transfers at this interface, the core can be used with simple SRAM but also SDRAM or DDR SDRAM. The core can be delivered with a standard SRAM controller; a suitable SDRAM controller is separately available. The core has been optimized in order to minimize the amount and bandwidth of off-chip memory. A single frame needs to be stored and accesses are reduced to 1 read and 1 write per input sample.

The following sections describe the modules constituting the BA132MPEG4D core as depicted under Figure 1.

Header decoding

This module decodes compliant MPEG-4 VOL and VOP headers (short headers and data partitioning are not supported but the core can be customized to add these features).

Entropy decoding

The entropy decoder applies a Huffman decoding on both the motion vectors and the compressed pixels. This module uses pre-defined Huffman tables.

Texture decoding

This module decodes error frames when dealing with P-VOPs (motion compensated) or complete frames when dealing with I-VOPs.

The texture decoding works on block level (8x8) and is made of zigzag encoding, inverse quantization, AC/DC prediction and Inverse Discrete Cosine Transform (IDCT).

Motion compensation

This module is bypassed for Intra-coded pictures (I-VOP). For P-VOPs, it combines the so-called error picture (coming from the texture decoder) to the reference frame (stored in off-chip memory), using the movement information carried by the decoded motion vector. The motion compensation unit supports the definition of a single motion vector per macroblock (the 4MV mode is not supported).

Implementation data

The following table details implementation results of the BA132MPEG4E core on various FPGA technologies. The core is 100% RTL and ASIC technologies can also be mapped. Performance figures enable real-time decoding for all Simple Profile L1 to L5 levels.

Device	Logic ³⁾	# of Clk	Performance (MHz)	Needed Resource ³⁾	Troughput (Msamples/s) ¹⁾
Altera EP1S25C5 ²⁾	10900 LE's	1	65	90 M4K, 30 DSP Multipliers	25
Xilinx XC2V1500-4	5450 Slices	1	65	29 RAMB16, 30 MULT18x18	25

1) Results for typical compression, as measured on difficult video sequences

2) Estimated (contact us for latest figures)

3) Resources for single-stream decoding (contact us for multiple-stream implementations)

Pinout description

Name	I/O	Size	Comments
Global			
CLK	I	1	Clock
RESET	I	1	Global asynchronous reset
Command and Control Interface			
START	I	1	Start decoding command
DONE	O	1	End of decoding status
ERROR	O	1	Error status
ERRORCODE	O	16	Error code
Compressed Data Interface			
CSTRB	I	1	Compressed data strobe
CSTNUM	I	3	Compressed data stream id (0..7)
CD	I	8	Compressed data
CFULL	O	8	Compressed data not ready (1 signal per stream)
Pixel Interface			
PFULL	I	1	Pixel not ready
PD	O	8	Pixel data
PSTRB	O	1	Pixel strobe
Memory Interface (read queue)			
MRQFULL	I	1	Read request queue full
MRQPUSH	O	1	Push read request
MRQADDR	O	32	Read request address
MRQEMPTY	I	1	Read data queue empty
MRQPOP	O	1	Pop read data
MRQRD	I	32	Read data (16-word burst)
Memory Interface (write queue)			
MWQFULL	I	1	Write request queue full
MWQPUSH	O	1	Push write request
MWQADWD	O	32	Write request address and write data (16-word burst)

Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

- image processing
- communications
- consumer electronics
- industrial electronics.

Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order-reference: **BA132MPEG4D**

For additional information and other IP products contact:

Barco – Silex

e-mail: barco-silex@barco.com

<http://www.barcodesignservices.com>

or the local Barco Silex design centers:

Belgium

Scientific Park
Rue du Bosquet 7
1348 Louvain-la Neuve
+32(0)10/45.49.04

France

ZI Peynier- Rousset
Route de Trets Imm CCE
13790 Peynier
+33(0)44/216.41.06