

Multi-Port AHB SDR/DDR SDRAM Memory Controller BA312

FactSheet

SDRAM Interface Features

- Single Data Rate SDRAM and Double Data Rate SDRAM are supported.
- Compatible to JEDEC standard (JESD79C for DDR). The BA312 Controller fully supports Micron, Samsung and Infineon devices, among others.
- Operates at frequencies up to 200 MHz.
- Programmable CAS Latency: 2, 2.5 or 3 clock cycles.
- Automatically generates the SDRAM initialization sequence.
- Supports up to 14-bit address bus.
- Programmable row and column address bit widths up to:
 - 14-bit row address (max. 16k rows);
 - 11-bit column address (max. 2k columns);
 - 2-bit bank address (max. 4 banks).
- Memory data width can be configured to 8 or 16 bits for double data rate SDRAM and to 16 or 32 bits for single data rate SDRAM. Larger bus widths will be supported in the next versions of the IP.
- Supports up to 4 chip select signals in the current version.
- Burst lengths of 1, 2, 4 or 8 are supported for single data rate SDRAM.
- Burst lengths of 2, 4 or 8 are supported for double data rate SDRAM.
- Supports Auto Refresh mode, Self Refresh mode and power-down mode.
- Supports all power-saving features (PASR, TCSR & Deep Power Down) for Mobile SDRAM.
- NOP, READ, WRITE, ACTIVE, AUTO REFRESH, PRECHARGE and BURST TERMINATE commands fully supported.
- Auto Precharge option supported.
- The following parameters are programmable: tRAS, tRCD, tRRD, tRP, tWR, tWTR, tXSR, and tRC.
- Supports 4 open banks. The bank management is optimized to minimize the host bus latency.
- SDRAM module serial presence detect not supported.
- Able to interface with an EBI (External Bus Interface).

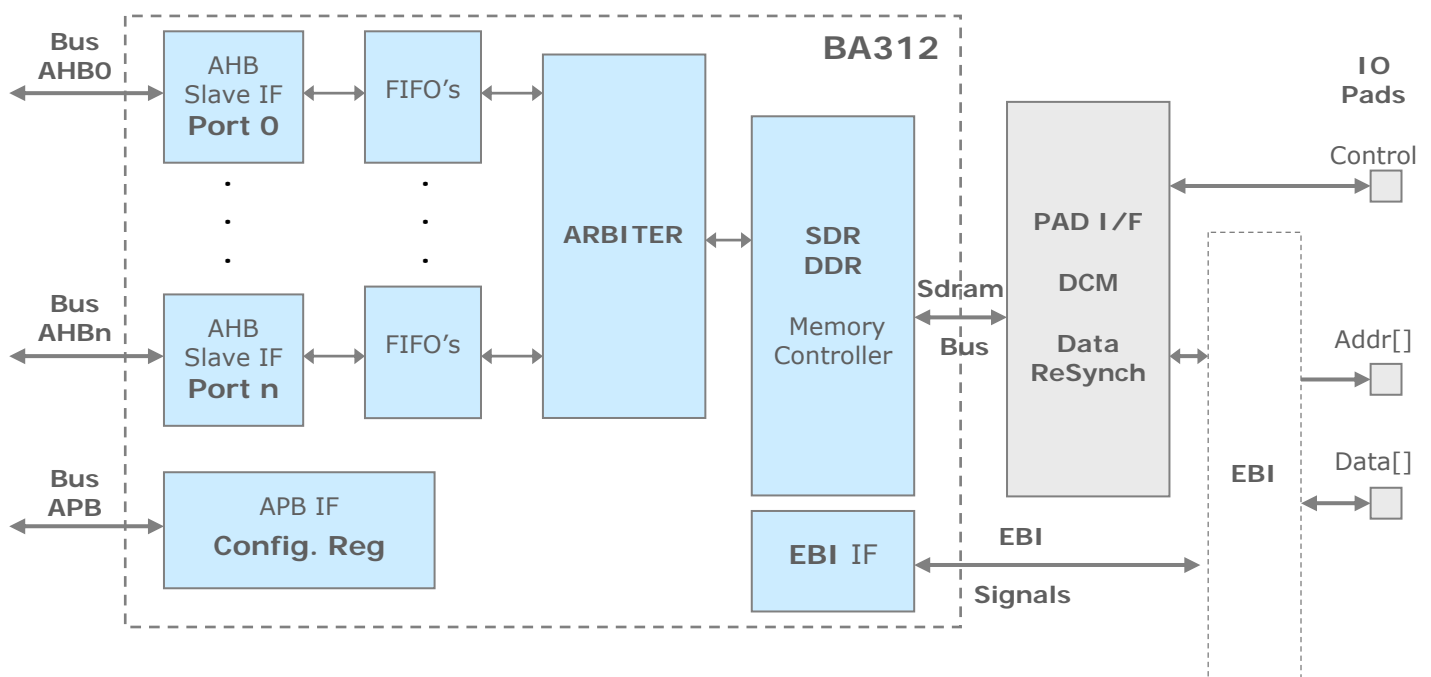


Figure 1 - BA312 Block Diagram

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AMBA AHB Interface

- AMBA AHB 2.0 bus-compatible;
- Does not generate SPLIT, RETRY & ERROR responses on the AMBA bus;
- Supports all types of AMBA bursts;
- Supports AHB data width of 32 (+ narrow access on 16 or 8 bits);
- Supports AHB address width of 32 bits;
- Management of two independent AHB ports;

General Description

The DDR-SDRAM Controller is AMBA AHB2.0 bus-compatible and can support both single data rate (SDR-SDRAM) and double data rate (DDR-SDRAM) devices. All power-saving features (PASR, TCSR & Deep Power Down) for Mobile SDRAM are also supported.

On the host side, the DDR-SDRAM Controller is interfaced through one, two or more independent AHB slave interfaces, referenced as 'ports' in the present document. The number of ports can be easily extended to 3 or 4, according to the application requirements.

For write operations, each AHB port has dedicated buffers to stack up the commands and the associated data. Any read command is treated with the highest priority to minimize the latency on the AHB busses connected to the SDRAM controller ports.

All commands are managed by a common arbiter and sent to the SDRAM Controller. The SDRAM Controller is able to optimize the bandwidth when successive or concurrent operations are required : the Controller can manage up to 4 open banks and to interlace PRECHARGE, ACTIVE & READ/WRITE commands to different rows (PRECHARGE & ACTIVATE commands are inserted automatically during the data cycles). Some waveforms related to different cases are given in section 7.

The following parameters must be configured before synthesizing the SDRAM Controller IP to optimize the occupied area:

- Data Rate: Single or double;
- Memory Data Bus Width: 8, 16 or 32;
- Size of buffers.

Some other parameters can be configured via the APB interface:

- Number of rows, columns;
- SDRAM CAS Latency;
- SDRAM Burst Length;
- RBC (Row, Bank, Column) or BRC (Bank, Row, Column) Address Mapping;
- AUTO PRECHARGE feature.

Note: the SDRAM burst type cannot be configured because AHB bus does not support interleaved bursts.

In the case of the same set of external pins is shared with another memory controller (Static Memory Controller for instance), the BA312 is able to interface with an EBI (External Bus Interface).

One extra block including the DCM (Digital Clock Manager) and the entire logic to capture read data is used to interface the Memory Controller with an external SDRAM device. Depending of the technology (ASIC or FPGA) and the type of SDRAM (SDR or DDR), different solutions are possible.

Implementation Data

- Max. Frequency : > 200MHz (90 nm TSMC ASIC technology).
- Complexity (for 2 ports): 50kgates (+17kgates / additional AHB port).
- No wait state needed for AMBA write operations due to the use of separated command buffers. When all the buffers are full, the write operation is extended with insertion of wait states.
- A six-clock-cycles response is required for read operations from addresses corresponding to rows that already are active. Some more clock cycles must be added when accessing rows that are not active.
- High-performance bank management: banks are only opened or closed when necessary, access requests to the memory device(s) are chained, PRECHARGE & ACTIVATE commands are performed and are automatically inserted during data cycles to optimize the bandwidth.

- Read operation are treated with the highest priority.

Pinout description

On request

Silicon proven

- Atmel 0.18um,
- UMC 0.35um,
- TSMC 90nm,

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More Information

Order-reference: **BA312**

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