

# Single-Port AHB SRAM-NorFlash Controller

## BA313A

*Factsheet*

### Key Features

- up to 10 chip select lines, max. 16 MByte of address space for each device;
- individual 8, 16 or 32 bits data bus configuration for each line. Access to separate byte is possible in 16-bit mode, and access to separate byte or half-word in 32-bit mode;
- individual wait state configuration, from 0 to 31 cycles;
- Little endian architecture
- Byte lane control
- Programmable output enable and write enable delays
- Programmable bus turnaround
- Write protection
- Access type configuration : cs, ncs, or ncs & E
- Non multiplexed and multiplexed data bus
- 68-type or 80-type interface
- wait request signal and optional timeout feature for slow devices;
- Ready signal for NOR flash support;
- APB interface for register configuration;
- External Bus Interface (EBI) support;
- interrupt signal on timeout event.

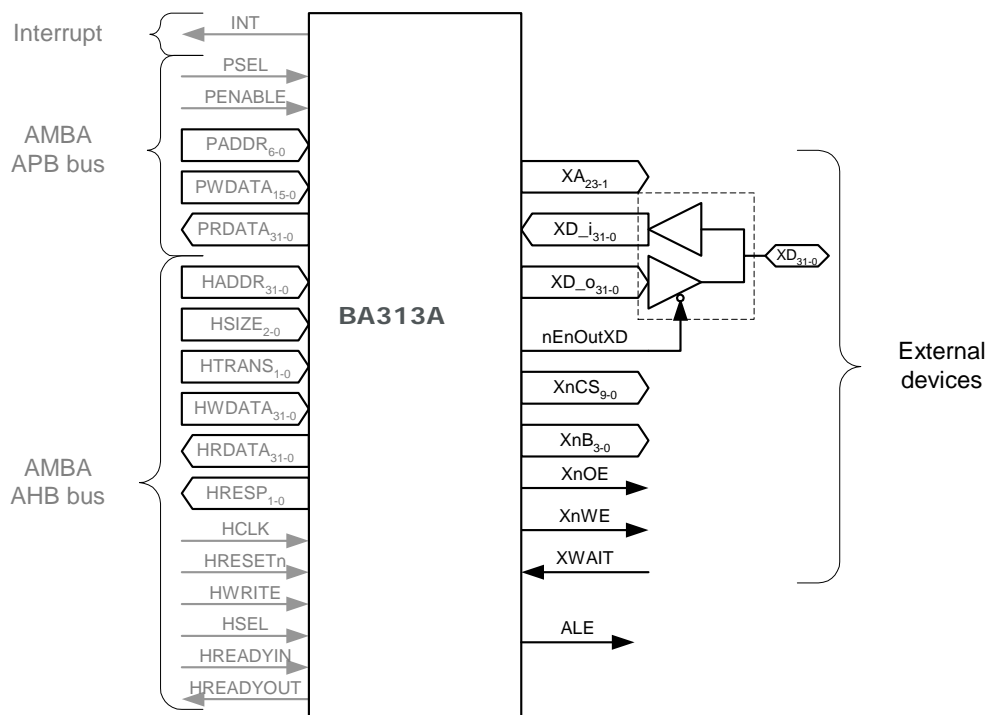


Figure 1 - BA313A – Input/output signals

## General Description

The BA313A is a AHB Slave Controller which provides interface to asynchronous external memory devices. It generates the control and address buses, and handles data bus buffering.

As an External peripheral Interface, the BA313A I/O channels can be configured in Motorola 68- or Intel 80-style protocols. In each configuration, there are several options like multiplexing (using the **ALE** signal to send the address and data) and CS polarity.

As a NOR Flash Controller, the BA313A generates Ready/Not Busy signals (XReady). The XReady input is resynchronized inside the BA313A. The XReady value is always observable through APB interface (XReady bit of SMCSTATUS register). Besides that, it is possible to trigger an interrupt on rising XReady edge. The interrupt must be enabled (RdyIntEn bit of SMCCONFIG register). When the interrupt occurred, the corresponding status bit is set (RdyIntStat bit of SMCSTATUS register). This bit (and the interrupt) can be cleared by writing a zero.

In the case of the same set of external pins is shared with another memory controller (NandFlash Memory Controller for instance), the BA313A is able to interface with an EBI (External Bus Interface).

## Pin Description – External device

Table 1 - External memory interface

| Pin                             | Dir. | Pol. | Description                                                                                                                                                                                                                                                                                                 |
|---------------------------------|------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| XA <sub>23-1</sub>              | out  |      | Address bus. The address bits are the same as the ASB bus, thus 32-bit devices should ignore XA <sub>7</sub> . Byte and half-word accesses are achieved with XnB signal. XnB <sub>0</sub> has the same functionality as XA <sub>0</sub> for 8-bit devices (see <b>Error! Reference source not found.</b> ). |
| XnB <sub>3-0</sub>              | out  | L    | Bytelane select. These signals select the individual bytes for the current R/W operation, for 16- and 32-bit devices.                                                                                                                                                                                       |
| XD <sub>i</sub> <sub>31-0</sub> | in   |      | Data input bus.                                                                                                                                                                                                                                                                                             |
| XD <sub>o</sub> <sub>31-0</sub> | out  |      | Data output bus.                                                                                                                                                                                                                                                                                            |
| nEnOutXD                        | out  | L    | Data output enable command for tri-state buffers.<br>0: output direction<br>1: input direction                                                                                                                                                                                                              |
| XnCS <sub>9-0</sub>             | out  | L    | Chip select.                                                                                                                                                                                                                                                                                                |
| XnOE                            | out  | L    | Output enable.                                                                                                                                                                                                                                                                                              |
| XnWE                            | out  | L    | Write enable.                                                                                                                                                                                                                                                                                               |
| ALE                             | out  | L    | Address Latch Enable.                                                                                                                                                                                                                                                                                       |
| XWAIT                           | in   | H    | Device not ready input signal. This signal, when asserted, requests additional wait cycles for the current R/W operation. The maximum number of additional wait cycles is set by a configuration register. This input is not resynchronized.                                                                |
| XReady                          | in   | H    | This signal is intended for Ready/Not Busy signal from Nor-Flash. This input is internally resynchronized.                                                                                                                                                                                                  |

### Maximum Frequency - (.13um ASIC technology)

- HCLK: 200MHz

### Deliverables

- Compiled model available on request for evaluation;
- Verilog RTL sources;
- TestBench;
- Documentation;

### Implementation Data

- 10kgates (Scan included) for controller alone,

### Maturity/Silicon-proven

- Silicon-proven with several implementations in different technologies

## Signals description

Refer to the datasheet document for a more detailed description.

## Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

- image processing
- communications
- consumer electronics
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## Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

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Deliverables include:

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- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

## More information

Order-reference: **BA313A**

For additional information and other IP products contact:

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