

Single-Port AHB NandFlashController

BA315A

FactSheet

Key Features

- 1 • Single-Port AMBA AHB 2.0 bus-compatible;
- 2 • Supports SLC & MLC Nand Flash memory devices;
- 3 • Generates Boot Sequence;
- 4 • Supports handshake signals to interface with an external DMA Controller;
- 5 • Error Correction: Reed-Solomon or Hamming
- 6 • All parameters programmable through APB Interface;
- 7 • Very low power consumption can be obtained by gating clock for ECC;
- 8 • Able to interface with an EBI (External Bus Interface);
- 9 • All data transfers are processed through an external buffer memory;
- Best trade-off performance/area by defining generic parameters before synthesis;

AHB Interface

- AMBA AHB 2.0 bus-compatible;
- Does not generate SPLIT, RETRY & ERROR responses on the AMBA bus;
- Supports all types of AMBA bursts;
- Supports AHB data width of 32 (+ narrow access on 16 or 8 bits);

Nand-Flash Interface

- Supports SLC & MLC Nand-Flash Memory Devices;
- Supports ONFI devices;
- Supports up to 5 address bytes;
- 8- or 16-bit data bus configuration;
- Supports up to 4 chip select signals;
- Supports up to 4kBytes page transfers;

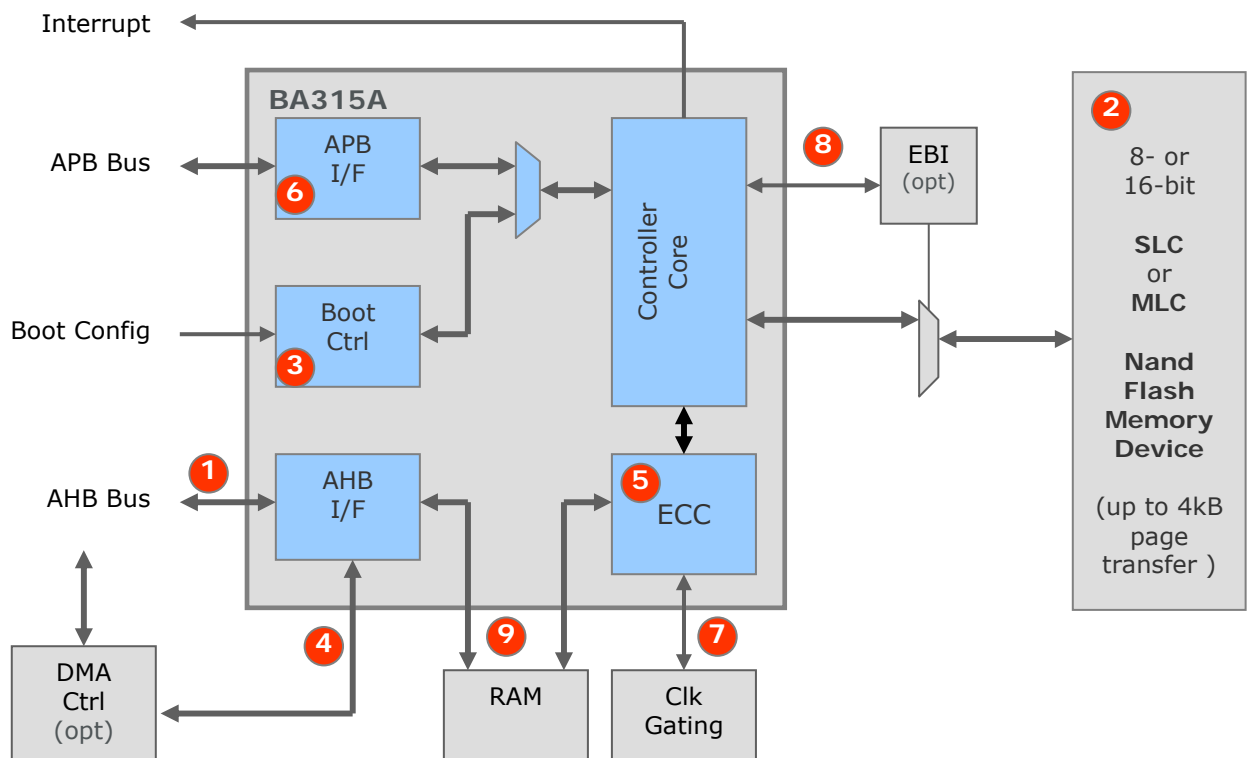


Figure 1 - BA315A Block diagram

General description

The BA315A is a configurable Single-Port AHB Nand-Flash Controller developed, validated & licensed by BARCO-Silex. It supports both SLC & MLC Nand-Flash memory devices in 8-bit or 16-bit configuration.

The AHB interface supports all kind of transfers. As the Nand-Flash memory device is slower than the AHB data bus, all data transfers are processed through an external buffer (embedded 32-bit RAM Block). Typically the size of the RAM is equal to the size of one nand-flash page (1, 2, 4 or 8 x 528-bytes). However, the controller is able to work efficiently with pages larger than RAM size.

The BA315A is able to boot on code located in nand-flash memory by automatically fetching the code (boot configuration defined by static input pins).

In the case of the same set of external pins is shared with another memory controller (Static Memory Controller for instance), the BA315A is able to interface with an EBI (External Bus Interface).

The BA315A can perform error detection & correction. Both Reed-Solomon and Hamming algorithms are available. All features related to ECC are listed in table 2 below.

According to the application requirements, the generic parameters listed in Table 3 can be configured before synthesis, allowing customers to make the best possible trade-off between performance and area.

Technical Description

Supported commands

The base sequence is made of seven steps (cmd1, cmd2, address, write data, cmd3, ready/busy, read data) which can be individually enabled and configured, so almost any sequence can be generated. The table below shows a non-exhaustive list of commands (ONFI command set has been used as example).

Sequence configuration							
Nand-flash command	Cmd1 (*)	Cmd2	Address	Write data	Cmd3	Ready/Busy	Read data
Read	-	00h	5 bytes	-	30h	Yes	Yes
Copyback read	-	00h	5 bytes	-	35h	Yes	-
Change read column	-	05h	2 bytes	-	E0h	-	Yes
Read cache (seq.)	-	-	-	-	31h	Yes	Yes
Read cache (random)	-	00h	5 bytes	-	31h	Yes	Yes
Read cache end	-	3Fh	-	-	-	Yes	Yes
Block erase (interleaved)	-	60h	3 bytes	-	D0h (D1h)	Yes	-
Read status	-	70h	-	-	-	-	Yes
enhanced	-	78h	3 bytes	-	-	-	Yes
Page program (interleaved)	-	80h	5 bytes	Yes	10h (11h)	Yes	-
Page cache program	-	80h	5 bytes	Yes	15h	Yes	-
Copyback prgm (interleaved)	-	85h	5 bytes	-	10h (11h)	Yes	-
Change write column	-	85h	2 bytes	Yes	-	-	-
Read ID	-	90h	1 byte	-	-	-	Yes
Read parameter page	-	ECh	1 byte	-	-	Yes	Yes
Read unique ID	-	EDh	1 byte	-	-	Yes	Yes
Get features	-	EEh	1 byte	-	-	Yes	Yes
Set features	-	EFh	1 byte	Yes	-	Yes	-
Reset	-	FFh	-	-	-	Yes	-

Table 1 – Supported commands

(*) The Cmd1 is useful for small block Nand-Flash using pointer operation (for example Samsung K9F5608). The command 00h, 01h or 50h can be issued before a page program sequence to set the pointer to 1st half array, 2nd half array or spare array.

Supported Devices

- 8- & 16-bit, SLC & MLC memory devices from Samsung, Toshiba, Micron or other providers.

Error-Correcting Code (ECC)

ECC		
Algorithm	Reed-Solomon	Hamming
User Data Bytes / Block	512	512 - fixed
Maximum number of Blocks	8	8
ECC Bytes / Block	10	3
Correction	4 byte errors	1 bit error
Detection	8 byte errors	2 bit errors
Write one 512-bytes Block	522 cycles	134 cycles
Read one 512-bytes Block	532 cycles	136 cycles
Read one 512-bytes Block + correction	1246 cycles	136 cycles

Table 2 – ECC Features

Generic Parameters

Generic Parameters	
Parameter	Description
g_reedsolomon	This parameter specifies whether the BA315P supports Reed-Solomon ECC
g_hamming	This parameter specifies whether the BA315P supports Hamming ECC

Table 3 - Generic Parameters

Clock Management

The clocks can be grouped into three clock domains as shown in Table 3. To reduce the power consumption in idle mode, ECC clock can be stopped.

Clock Domains		
Clock Name	Clock Domain	Description
HCLK	Core Controller	Main Clock
PCLK	APB Interface	APB Clock. PCLK & HCLK must be synchronous
ECC_CLK	ECC	Slower gated version (output signal ecc_clk_en) of HCLK

Table 4 – Clock Domains

Maximum Frequency - (.13um ASIC technology)

- HCLK: 200MHz
- ECC_CLK: 100MHz (Reed-Solomon)

Deliverables

- Compiled model available on request for evaluation;
- Verilog RTL sources;
- TestBench;
- Documentation;

Implementation Data

- 10kgates (Scan included) for controller alone,
- 3kgates (Scan included) for Hamming ECC module
- 27kgates (Scan included) for Reed-Solomon ECC module

Verification Flow

- Nand-Flash Device Interface verified with several models from Micron, Samsung, Toshiba...

Maturity/Silicon-proven

- Silicon-proven with several implementations in different technologies:
 - UMC 0.35um,
 - TSMC 90nm
- validation on FPGA (Virtex family)

Signals description

Refer to the datasheet document for a more detailed description.

Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

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- consumer electronics
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Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

More information

Order-reference: **BA315A**

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