

# AXI DDR2 SDRAM Controller

## BA316

FactSheet

### Key Features

- 1 • Supports AMBA 3 AXI protocol (32 or 64-bit Data Width);
- 2 • Supports SDR, DDR, DDR2, Mobile SDR & DDR memory devices (8, 16, 32 or 64-bit configurations);
- 3 • Best trade-off performance/area by defining generic parameters before synthesis;
- 4 • All parameters programmable through APB Interface;
- 5 • Clocking Ratio 1:1, 1:2 or 1:4 between AXI & SDRAM Interfaces;
- 6 • Very low power consumption can be obtained by gating several internal clocks;
- 7 • Able to interface with an EBI (External Bus Interface);
- > • Compliant with DDR PHY Interface Specification (DFI) version 1.0;

### AXI Interface

- Supports unaligned data transfers
- Supports multiple outstanding addresses;
- Out-of-order transaction completion;

### DDR/DDR2-SDRAM Interface

- Automatically generates the initialization sequence;
- Programmable row and column address bit widths up to: 16-bit row/ 11-bit column/ 3-bit bank address;
- Supports up to 4 chip select signals;
- All burst lengths supported: 2,4, 8 for DDR; 4, 8 for DDR2;
- Auto Refresh, Self Refresh & Power-Down modes supported;
- Auto Precharge options supported
- SDRAM module serial presence detect not supported

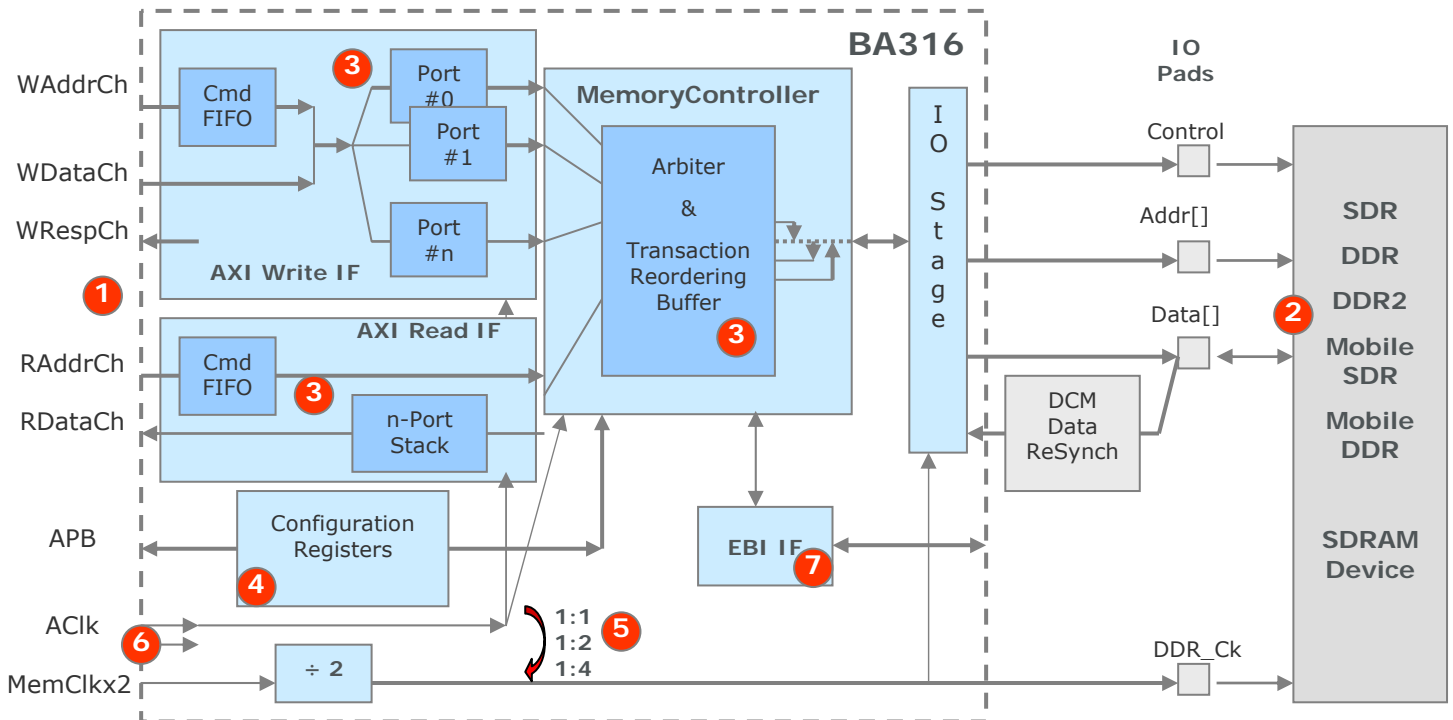


Figure 1 - BA316 Block Diagram

## General description

The BA316 is a configurable AXI DDR/DDR2-SDRAM Memory Controller developed, validated & licensed by BARCO-Silex. It supports both Single Data Rate (SDR) and Double Data Rate (DDR/DDR2) SDRAM devices and all power-saving features for Mobile SDR/DDR-SDRAM devices.

Entering AXI Write & Read Commands are stacked up in separated Command Buffers (Write & Read Acceptance Capabilities) while corresponding data are stacked up into dedicated buffers. Transactions with different ID Tags are treated through separated "Virtual Ports" with automatic allocation of buffers. According to the application requirements, the generic parameters listed in Table 1 can be configured before synthesis, allowing customers to make the best possible trade-off between performance and area.

All commands are managed by a common arbiter and SDRAM Controller. The SDRAM Controller is able to optimize the bandwidth when successive or concurrent operations are required: the controller can manage up to 4 (8 for DDR2) open banks and to interlace PRECHARGE, ACTIVE & READ/WRITE commands to different rows (PRECH & ACT commands are automatically inserted during data cycles).

## Technical Description

### Generic Parameters

Generic Parameters	
Parameter	Description
AxiWidth	AXI Data Bus Width (32 or 64)
SdramDataWidth	SDRAM Data Bus Width (8, 16, 32 or 64)
Write Acceptance Capability	Maximum number of active pending AXI write transactions that the BA316 can accept
NbWritePorts <i>or</i> Write IDTag Capability	Maximum number of interleaved AXI write transactions (with different ID tags) that the BA316 can accept.
Read Acceptance Capability	Maximum number of active pending AXI read transactions that the BA316 can accept
NbReadPorts <i>or</i> Read IDTag Capability	Maximum number of interleaved AXI read transactions (with different ID tags) that the BA316 can accept.
NbBytesWDataFifo	Write Data FIFO Size (in bytes) / Port
NbBytesRDataFifo	Common Read Data FIFO Size (in bytes)
ReorderDepth	Depth of Reordering Transaction FIFO

Table 1 - Generic Parameters

### Programmable Parameters

Programmable Parameters through APB Interface	
Parameter	Description
Device	Type of Memory Device: SDR, DDR, DDR2, Mobile SDR, Mobile DDR Number of addr bits for Row and Column addressing, Burst Length, CAS Latency, ...
Timing	Active, Precharge, R/W, Refresh Timing Parameters, AUTO PRECHARGE features, ...
DataRate	Number of Memory Data Transfers per AXI Clock Cycles (ClockRatio x 2).

Table 2 - Programmable Parameters

## Clock Management

The clocks can be grouped into three clock domains as shown in Table 3. To reduce the power consumption in idle mode, several derived clocks can be stopped.

Clock Domains		
Clock Name	Clock Domain	Description
<b>ACLK</b>	<i>AXI IF + Core Controller</i>	AXI Master Clock + derived gated clocks
<b>PCLK</b>	<i>APB Interface</i>	APB Master Clock. PCLK & ACLK can be asynchronous
<b>ClkMem2x (in) DDR_Ck (out)</b>	<i>Device Interface</i>	Input clock ClkMem2x must be clocked at double rate of the external memory DDR_Ck ( <b>DDR_Ck = ClkMem2x/2</b> )

Table 3 – Clock Domains

## Maximum Frequency - (90nm TSMC ASIC technology)

- ACLK: > 266MHz (without any special effort)
- ClkMem2x/DDR\_Ck: > 666MHz (DDR\_Ck=333MHz)

## Supported Devices

- DDR -200, -266, -333, -400 are supported (values in Mbps) with ACLK = DDR\_Ck
- DDR2 -400, -533 are supported (values in Mbps) with ACLK = DDR\_Ck
- DDR2 -400, -533, -667 are supported (values in Mbps) with ACLK = DDR\_Ck/2

## Power Management

- Supports all power-saving features (PASR, TCSR & Deep Power Down) for Mobile SDRAM
- Very Low Power Consumption can be obtained by gating several internal clocks in the ACLK clock domain (Enable signals available at the output of the BA316).
- Time-out counter to automatically enter/exit power-down mode;

## Deliverables

- Compiled model available on request for evaluation;
- RTL/VHDL/Synchronous Design;
- TestBench;
- Documentation;

## Implementation Data

- 90kgates (Scan included) for high-performant solution
- between 50k & 80kgates (Scan included) for medium-performance solutions

## Verification Flow

- AXI Interface verified with DesignWare Verification IP for AMBA3 AXI Protocol from Synopsys,
- SDRAM Device Interface verified with several models from Micron, Samsung, Infineon...

## Maturity/Silicon-proven

- Upgrade of the **BA312** (Multi-Port AHB DDR-SDRAM Memory Controller) that is silicon-proven with several implementations in different technologies (Atmel 0.18um, UMC 0.35um, TSMC 90nm)
- validation on FPGA (Virtex family)

## Supported Devices & Configurations

As shown in Table 4, different clock ratios between AXI & external memory device interfaces are supported.

Supported devices & configurations								
Host Config		Device Config		SDR	DDR		DDR2	
AXI Width (bits)	SDRAM Width(bits)	Burst Length (data)		Clock Ratio = Data Rate	Clock Ratio	Data Rate	Clock Ratio	Data Rate
32	8	4		1, 2, 4	1, 2	2, 4	1, 2	2, 4
32	8	8		1, 2, 4, 8	1, 2, 4	2, 4, 8	1, 2, 4	2, 4, 8
32	16	2		1, 2	1	2	-	-
32	16	4		1, 2, 4	1, 2	2, 4	1, 2	2, 4
32	16	8		1, 2, 4	1, 2	2, 4	1, 2	2, 4
32	32	1		1	-	-	-	-
32	32	2		1, 2	1	2	-	-
32	32	4		1, 2	1	2	1	2
32	32	8		1, 2	1	2	1	2
32	64	1, 2, 4, 8		1	-	-	-	-
64	8	8		1, 2, 4, 8	1, 2, 4	2, 4, 8	1, 2, 4	2, 4, 8
64	16	4		1, 2, 4	1, 2	2, 4	1, 2	2, 4
64	16	8		1, 2, 4	1, 2	2, 4	1, 2	2, 4
64	32	2		1, 2	1	2	-	-
64	32	4		1, 2	1	2	1	2
64	32	8		1, 2	1	2	1	2
64	64	1, 2, 4, 8		1	-	-	-	-

Notes:

- DR (SDRAM Device Transfer Data Rate) is the number of data transfers that are performed from/to the SDRAM device per AXI Clock Cycle;
- Supports Micron, Samsung and Infineon devices, among others;

Table 4 - Supported Configurations

## Signals description

Refer to the datasheet document for a more detailed description.

## Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Belgian Barco group.

Barco Silex offers a complete portfolio of high-end design services, from ASIC/FPGA design to advanced SoC/SoPC based system development, IP-core design and board design in the fields of:

- image processing
- communications
- consumer electronics
- industrial electronics.

## Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, standardized image processing and encryption functions.

All these IP cores have been designed and fully validated by Barco Silex and are hardware proven, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL Code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

## More information

Order-reference: **BA316**

For additional information and other IP products contact:

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