

# ARINC 429 – DO-254 Compliant BA511

FactSheet

## Key Features

### Applicable Standards:

- Supports ARINC 429 standard part 1, 2 and 3
- Developed according to RTCA/DO-254 ED-80 guidance ( DAL A criteria)

### Technical features:

- Simple asynchronous CPU interface
- Supports up to 32 ARINC 429 inputs and 16 ARINC 429 outputs
- Independent channel configuration via the CPU interface
- 63 word buffer (FIFO) for each ARINC 429 input channel
- 31 word buffer (FIFO) for each ARINC 429 output channel
- FIFO Overflow, Parity error, Frame error

### Configuration support per channel:

- Low speed (LS, 12.5KHz) or high speed (HS, 100 KHz) mode
- Disable/Enable

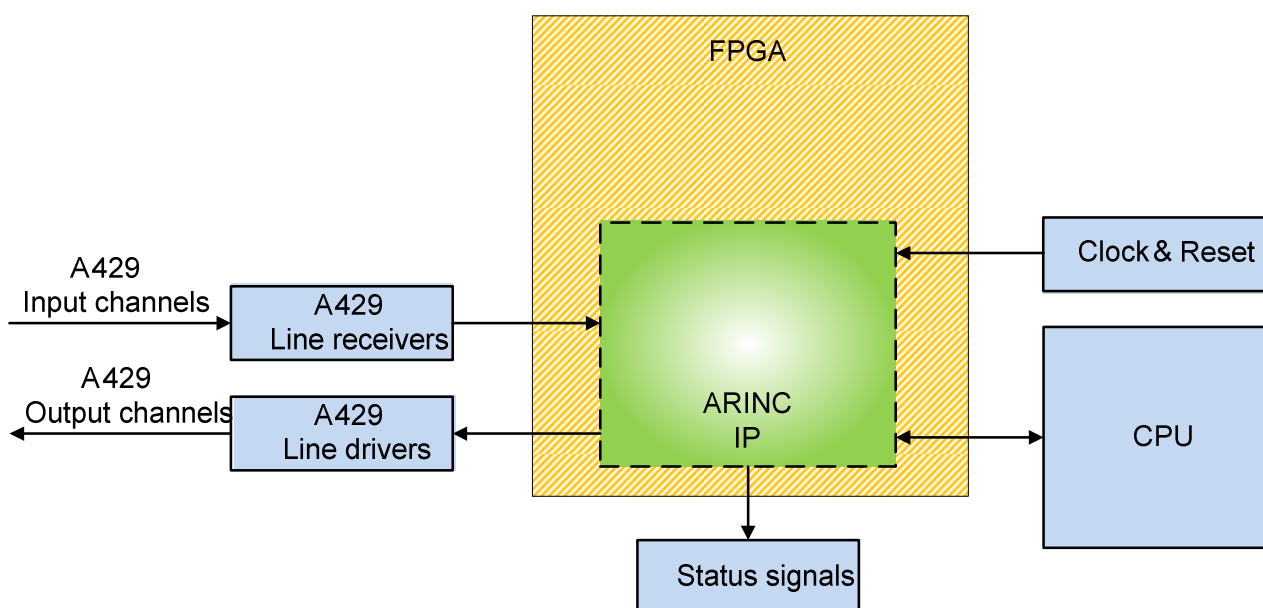


Figure 1 – BA511 integration diagram

Version 1.6

## General description

The BA511 is a multi-channel ARINC 429 transmitter and receiver core for serial communication in airborne applications. The BA511 is developed, validated & licensed by BARCO-Silex.

The BA511 has been developed according to the RTCA/DO-254 ED-80 guidelines. These guidelines are required by the Airworthiness Certification Authorities (EASA and FAA) for hardware developments that need to be certified for the use in commercial aircraft equipments.

The BA511 incorporates a simple basic asynchronous CPU interface which can easily be connected to your required interface. Each individual channel can be configured according to your specifications.

Each channel contains a specific buffer (FIFO), which are incorporated in the BA511. This allows efficient data transfer between the CPU and the BA511.

## Data items and documentation

### ***Deliverables***

- VHDL RTL sources compliant to the BARCO coding standard
- Functional verification test benches obtaining 100% code coverage
- Simulation and implementation scripts and logs in order to regenerate the same functional behavior
- Implementation results

### ***Documentation required for RTCA/DO-254 certification***

- Delivered Documents (**part of the IP package deliverables**):

#### Certification Liaison Process

- Plan for Hardware Aspect of Certification (PHAC)
- Hardware Accomplishment Summary

#### Hardware Development Process

- Requirements capture
- Conceptual design data
- Detailed design data
- Datasheet

#### Hardware Verification and Validation Process

- Traceability Matrices
- Hardware Verification Procedures
- Verification Reports

#### Hardware Configuration Management Process

- Hardware Configuration Index
- Hardware Environment Configuration Index

- Available Documents (**for audit purpose only, not part of the IP package deliverables**):

#### Hardware Planning Process

- Hardware Development Plan
- Hardware Validation and Verification Plan (HVVP)
- Configuration Management Plan
- Hardware Process Assurance Plan

#### Hardware Verification and Validation Process

- All reviews, audits and corresponding checklists

#### Hardware Process Assurance Process

- Audit report
- Records

## Implementation Data

Device	Description	System Clock		Needed Resource
Actel PROAsic3 A3P1000	* 8 Rx channels * 4 Tx channels * CPU interface	50	MHz	* 6500 tiles * 6 memory blocks (4,608-bits block)
Actel PROAsic3 A3P1000	* 32 Rx channels * 16 Tx channels * CPU interface	50	MHz	* 19874 tiles * 20 memory blocks (4,608-bits block)
Altera Cyclone III EP3C16U484C6	* 32 Rx channels * 16 Tx channels * CPU interface	50	MHz	* 10573 LE * 81,920 bits

## Hardware Design Life cycle Process

The hardware design life cycle process described in RTCA/DO-254 ED-80 has been applied.

## Service Experience

The BA511 is derived from ARINC429 modules that have been integrated in at least 3 different types of cockpit video displays, implemented in different FPGAs, for which some displays were granted for TSO and ETSO certification (DAL-A and DAL-B).

## Signal description

Refer to the datasheet document for a more detailed description.

Pin Name	Dir.	Size	Active edge	Description
<b>Global Interface</b>				
ClkSys	I	1	-	Global clock (Rising edge only)
nRst	I	1	low	Global asynchronous reset
<b>CPU Interface</b>				
Data_in	I	32	-	CPU Data input
Addr	I	8	-	CPU Address
nRE	I	1	low	Read Enable
nWE	I	1	low	Write Enable
nCS	I	1	low	Chip Select
Data_out	O	32	-	CPU Data output
<b>ARINC429 Interface</b>				
A429_TxA	O	16	-	ARINC Tx line A
A429_TxB	O	16	-	ARINC Tx line B
A429_RxA	I	32	-	ARINC Rx line A
A429_RxB	I	32	-	ARINC Rx line B
<b>Status Interface</b>				
A429HiSpd_Out	O	1	high	ARINC Tx Speed
A429TxStat	O	1	high	ARINC Tx Status
A429RxStat	O	1	high	ARINC Rx Status

## Barco Silex overview

Barco Silex is a micro-electronic design house located in Belgium and France belonging to the Barco group. It has 15 years of industrial experience in the ASIC and FPGA markets and offers you long term support and continuity.

Barco Silex has established a solid reputation in the development of DO-254 certifiable HW design date. Numerous FPGAs and ASICs have been developed for ETSO and TSO certified products from DAL-D towards DAL-A.

Starting from your upper level requirements (board requirements), we provide all services needed to create the necessary hardware design life cycle data according to a DO-254 requirements process.

We achieve this by means of a broad suite of development and verification tools, a state-of-the art knowledge about the latest ASIC and FPGA technologies and excellent relationships with those partners. This is why our services are valued by industry leading professionals worldwide.

Combining high-end know-how in design and verification processing, custom design capabilities (ASIC/FPGA/DSP/IP) and a thorough experience of the DO-254 recommendations, the company delivers high-quality custom-built DO-254 compliant VHDL design solutions.

## Barco Silex IP products

Barco Silex design expertise is also made available through a wide portfolio of IP products, with a strong focus on high performance, reliability, life cycle guarantee and quality. All these IP cores have been designed and fully verified by Barco Silex, which guarantees high IP quality as well as best support during your integration phase.

Deliverables include:

- RTL code or netlist (depending on license type)
- Functional simulation testbench
- Synthesis script
- Full documentation (depending upon the required quality standard)

For some of them, we can also provide you with simulation models and a design kit.

These "off the shelf", high quality IP cores provide you with the fastest and most efficient way of integrating complex functionalities on FPGAs or ASICs, while meeting short time to market constraints.

## More information

Order-reference: **BA511**

For additional information and other IP products contact:

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