

# AHB Multi-Channel DMA Controller

## BA612A

FactSheet

### Key Features

- 1 • AMBA AHB-lite compliant DMA transfers;
- 2 • Supports multiple transfer types: memory to memory, peripheral to memory, memory to peripheral;
- 3 • Number of DMA channels configurable;
- 4 • Supports Basic, Auto-request & Ping-Pong Transfer Modes;
- 5 • Low gate count solution with channel parameters stored in system memory:
  - Programmable burst length for each channel;
  - Programmable transfer width for each channel;
  - Programmable transfer type for each channel;
  - Programmable transfer mode for each channel;
  - Programmable transfer size for each channel;
  - Source & Destination addresses.
- 6 • All other parameters programmable through APB Interface;
- 7 • Fixed priority or round-robin scheme;
- Best trade-off performance/area by defining generic parameters before synthesis;

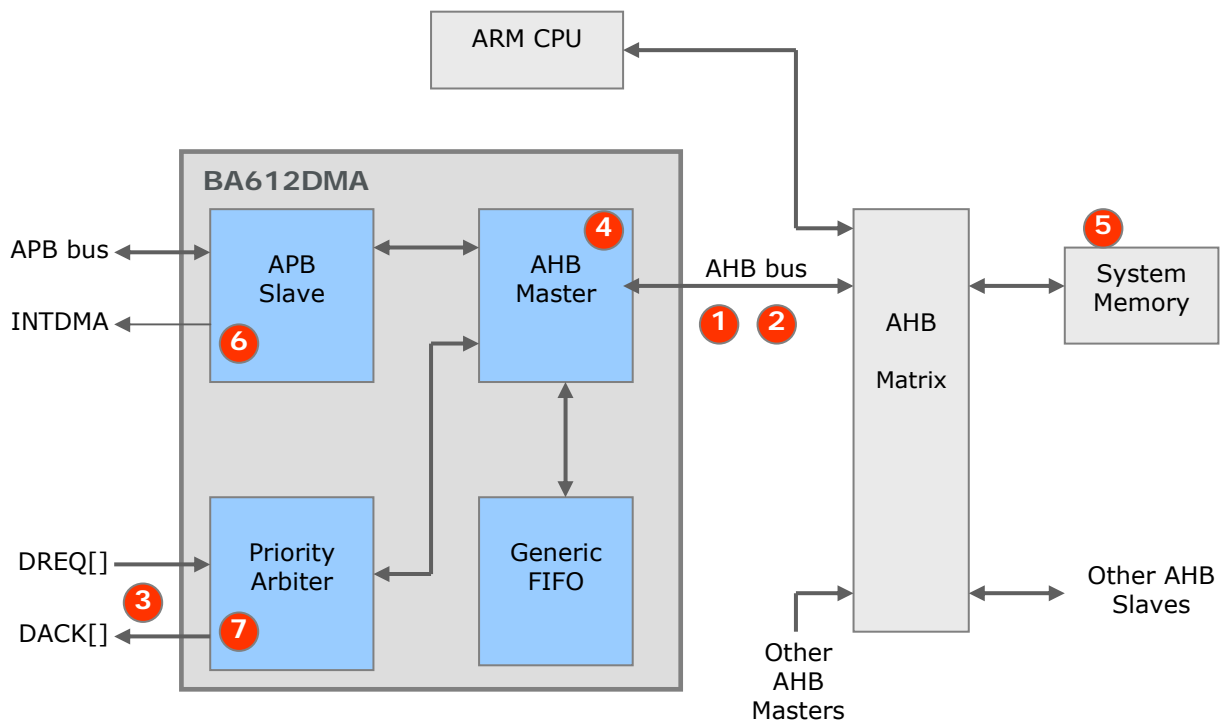


Figure 1 – BA612A Block diagram

Version: 1.0

## General Description

The BA612A is a configurable AHB-lite Multi-Channel DMA Controller developed, validated & licensed by BARCO-Silex. The BA612A is a low gate count DMA Controller which is able however to perform high-throughput DMA transfers. Following transfer types are supported: memory to memory, peripheral to memory, memory to peripheral.

The BA612A supports three transfer modes: Basic, Auto-Request & Ping-Pong transfer modes. In all cases, one DMA Block transfer of Nw words is splitted into Nb DMA Burst transfers (with  $Nb=Nw/BL$ ). The Burst Length (BL) is programmable separately for each channel.

Any DMA Burst transfer is executed as follows:

- The DMA Controller downloads channel parameters from the system memory if needed (when executing alternate Burst Transfers on different channels or starting a new Block transfer),
- One burst of data is transferred from the source into the internal fifo,
- Data stored in the internal Fifo are transferred to the destination,
- Arbitration is done after each Burst transfer,
- An interrupt is generated when the entire DMA Block transfer of Nw words is terminated,
- If NW is not a multiple of BL, the length of the last burst is adapted,
- If needed (when the Arbiter has granted the bus to execute a Burst transfer on another channel), the DMA Controller stores the updated channel parameters into the system memory.

In Basic Transfer Mode, a Block is transferred by executing previous Burst sequence each time the DMA Controller receives a DMA Request.

In Auto-Request Transfer Mode (for large data transfers), only one DMA Request is needed to execute the entire Block transfer. In this mode, the DMA Controller generates automatically next DMA Requests until the DMA Block transfer is completed.

In Ping-Pong Transfer Mode, 2 sets of parameters (primary & alternate) can be used. The DMA Controller switches automatically between primary and alternate settings.

According to the application requirements, the generic parameters listed in Table 4 can be configured before synthesis, allowing customers to make the best possible trade-off between performance and area.

## Technical Description

### Channel Control Structure

The control structure related to each channel is made up of three 32-bit registers which are stored in system memory.

Channel control structure in System Memory	
Register	Description
Configuration Ch_#i	This register specifies Transfer_Type, Transfer_Mode, Burst Length, Transfer Width, Number of Words parameters for Channel#i
Source Address Ch_#i	This register specifies the Source End Pointer for Channel#i
Destination Address Ch_#i	This register specifies the Destination End Pointer for Channel#i

**Table 1 – Channel Control structure in System Memory**

The Number of Words parameter is updated after each Burst Transfer if needed.

## APB Configuration Registers

Main configuration registers are accessed through the APB Interface.

APB Configuration Registers		
Register	Width	Description
Priority Reg.	1	Defines while Fixed or Round-Robin priority scheme is used
Configuration Registers	Some bits / Channel	Several configuration registers define while channels & interrupts are enabled
Status Registers	Some bits / Channel	Several Status registers provide information related to: Pending requests, Error, End of Transfer
Base Address	32	This register specifies the Base Address of the Channel Control Structure mapped into the System Memory.

Table 2 – APB Configuration Registers

## Generic Parameters

Generic Parameters	
Parameter	Description
g_Depth	This parameter specifies the FIFO size: 2, 4, 8 or 16 x 32-bit
g_Channel	This parameter specifies the number of channels in use.

Table 3 - Generic Parameters

## Clock Management

The clocks can be grouped into two clock domains as shown in Table 4.

Clock Domains		
Clock Name	Clock Domain	Description
HCLK	Core Controller	Main Clock
PCLK	APB Interface	APB Clock. PCLK & HCLK must be synchronous

Table 4 – Clock Domains

## Maximum Frequency - (90nm ASIC technology)

- HCLK: 200MHz

## Deliverables

- Compiled model available on request for evaluation;
- Verilog RTL sources;
- TestBench;
- Documentation;

## Implementation Data - 90nm TSMC

Gate Count	
Function	Gate Count
Core	4500 gates
Channel	200 gates per Channel
Fifo	500 gates per 32-bit word

Table 5 – Gate Count

Configurations			
Description	Number of channels	FIFO size	Gate count
Minimal configuration	2 channels	2 words	6k gates
Typical configuration	12 channels	8 words	11k gates
Maximal configuration	32 channels	16 words	19k gates

Table 6: Configurations

## *Maturity/Silicon-proven*

- Silicon-proven with several implementations in different technologies
- validation on FPGA (Virtex family)

## Signals description

Refer to the datasheet document for a more detailed description.

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- Synthesis script
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## More information

Order-reference: **BA612A**

For additional information and other IP products contact:

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